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Volume 7, Issue 2



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# Selection, Analysis and Development of Greenfield Sites for 300 mm Fabs

by Daren Dance and David Lauben, WWK Danny Lam, FHI Research.com Inc.

he semiconductor industry emerged from one of the most severe downturns in its history in 1999 with a worldwide growth rate of 19%, followed by a projected growth rate of about 38% in 2000. 2001 will in all likelihood see growth rates of more than 30% again as the industry continues to expand. Capacity utilization, similarly, has risen from a low of 81.6% during 3Q98 to 95.5% in 2Q00. Figure 1 shows these trends.



Figure 1. Capacity utilization rose from a low of 81.6% during 3Q98 to 95.5% in 2Q00. (Source: SIA, IC Insights)



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Subscription Information

Published Quarterly \$59.00/year in the U.S. \$69.00/year outside the U.S.

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## Wright Williams & Kelly Forms **New Contract Software Development Group**

December 12, 2000 Wright Williams & Kelly (WWK) announced today the release of COOL Fusion<sup>™</sup>, the first offering from its recently announced strategic alliance with Five Star Consulting. Additionally, WWK announced the formation of a new contract software development group to support COOL Fusion<sup>TM</sup> and other custom development projects. COOL Fusion<sup>™</sup> is a powerful user interface that allows direct and indirect capital equipment sales forces to quickly configure their products and generate pricing, throughput, and cost of ownership (COO) reports.

COOL Fusion<sup>™</sup> is based on a standard library of software objects that allow WWK to quickly customize the user interface to the customer's specific needs. Typical objects include user log-in, customer identification, equipment type, user defined input fields, and links to data tables and calculation engines. Data and calculation engines, such as TWO COOL® COO software, can be provided by the client's domain experts or by WWK.

During the development of this reusable sales platform, WWK found that many of their client's calculation engines were spreadsheet (Excel<sup>TM</sup>) based. In order to eliminate the need for additional software packages to operate COOL Fusion<sup>™</sup>, WWK developed a process by which spreadsheets can be automatically converted to runtime objects. These objects maintain their functionality but no longer require a separate spreadsheet program to operate. This development opens a very large opportunity to clients who want to distribute spreadsheet based programs with higher security and without the need to consider the impact of multiple spreadsheet versions and environments.

"Over the past three months our strategic alliance has yielded some very powerful tools to provide quick turn, custom software development to our clients," states David Jimenez, President of WWK. "While COOL Fusion™ promises to provide a tremendous value-add to our clients' sales forces, there may be even a larger benefit in our spreadsheet conversion platform. Just think how many spreadsheet based financial and engineering programs are distributed each year with little or no control once they are out of the hands of the developer."

One estimate of the demand for new fab sites, based on forecasted semiconductor industry capital spending,<sup>[1]</sup> is illustrated in Figure 2. During previous upturns, this level of growth and capacity utilization would have resulted in frenzied activity by companies seeking to find new fab sites and adding new capacity that would be "on stream" by 2003 or 2004 to meet anticipated demand. However, most companies have not done so during this upturn.



Figure 2. The demand for new fab sites, based on forecasted semiconductor industry capital spending. Note: Capital spending is likely to fall lower than this forecast in 2003 when the industry is expected to hit a slump.

Companies cut back severely on site analysis, development and selection activities as a result of the severe, double-dip slump between 1996 and 1998. At present, only one semiconductor company in the world can be said to have preserved its global site analysis, selection and development capabilities at pre-downturn levels, and have an "inventory" of viable sites for 200 mm fabs. Hence, capacity needs during this upturn, rather than being met by solid, well-funded, long-term site development programs, have been created by ad hoc measures. These include integrated device manufacturers (IDMs) using outsourcing strategies, purchasing unneeded fab shells from other vendors and filling them with equipment, and heavily investing in technological upgrading of existing fabs rather than building greenfield capacity. These were practically unthinkable in previous years but a necessary measure for the industry to conserve cash.

While ad hoc measures have been able to fill the need for 200 mm fab sites, no company has invested in developing good 300 mm greenfield fab sites. In all likelihood, when the industry finally determines that they have hit a capacity wall that can only be overcome by the addition of greenfield sites, sites for 300 mm fabs will be chosen not because the site is good, but because of expediency. Many of these sites will be sub-optimal both in terms of profitability and risks. The purpose of this article is to look at some of the technological and market changes that have occurred since the last upturn; to look at how these changes might impact the analysis, selection and development of greenfield sites; and how we have shortened the cycle time needed to bring a candidate greenfield site on stream using a set of software tools and techniques developed during the past three years.

### Lessons from the last upturn

The upturn that ended in 1995 was a defining moment in the semiconductor industry. For the first time, the average cost of a new fab surpassed \$1 billion, causing many sites that were marginally qualified in previous competitions to become decidedly unqualified. At these investment levels, the sheer cost and risks of failure, or normal teething problems encountered in any major construction project, become prohibitively expensive. From a company perspective, the lesson learned is that the cost of bringing an unqualified site in a remote location rapidly eliminates the benefits from even lavish government incentives. What appeared to be extremely good financial incentives — as much as 50 cents on the capital dollar invested — did not make up for the costs or risks involved.

At the same time, governments and communities have also learned bitter lessons that even the best companies can be severely impacted by an industry downturn. For a democratic government that is accountable to an electorate, problems with fab programs that put hundreds of millions of tax dollars at risk can rapidly turn an apparently successful industry recruitment program into a severe political liability. Accordingly, both industry and governments have learned that semiconductor programs, even if they are well conceived and executed, involve risks on both sides. It is not at all certain that rewards will follow just because one or the other party is willing to invest a few billion dollars in a program.

Despite these caveats, there are indeed successful programs. Singapore and Dresden are two examples of locations that have become successful in this industry. Assuming that there are two capable and competent partners, the single common factor that makes semiconductor industry programs successful involves a long-term commitment by the industry and government partners to make the program work over the long haul. This commitment must be supported by industry (not just one company), all levels of a candidate site's government, and the local business community. Once made, this commitment is firm, unwavering and sufficiently strong to weather not only short-term problems, but also such catastrophic events as a double-dip slump as experienced during the last industry downturn.

Beyond the necessary commitment by the parties, there is a second key factor. Good semiconductor programs are about "win-win" deals. From the start, they must be crafted as mutually beneficial. Without this, there is no foundation to allow cohesion or to maintain the necessary levels of commitment. A program that is one-sided is unlikely to work over the long haul. Typical problematic ones, for example, are those that involve substantial cash subsidies from a government, with little risk-sharing from the company, and no prospect for a positive return on investment for the governments or communities involved.

### New technology, new needs

As the industry transitions to 300 mm, the cost of a new fab built between 2002 and 2003 will likely rise to \$2 billion. As costs rise and technical specifications tighten, industry needs are rapidly fragmenting, with the needs of a 200 mm trailing edge foundry being drastically different from those of a 300 mm state-of-the-art facility that manufactures a high-value-added product like DSPs.

The high concentration of capital in 300 mm facilities leads to much more stringent requirements for business interruption risks, vibration, and pool of labor quality. Company requirements are also fragmenting. The needs of a flash memory facility drastically differ from those of a DSP or microprocessor manufacturing facility.

Candidate sites have also changed greatly. Some greenfield fab sites in the Pacific Rim that were formerly strong candidates have yet to recover from the Asian crisis and are unlikely to be serious contenders in the near future. Eastern Germany, in the meantime, has greatly improved its facilities and infrastructure. Should the euro remain at its present depressed levels, it can potentially make Europe a preferred location for new fab sites. China, the perennial promising candidate, has two solid facilities — Tianjian (Motorola) and Shanghai (NEC) — that are to begin or have begun production. The proposed pure-play foundry joint ventures in China have all the indications of being winners. On the other hand, the booming economy in the United States means that there are few locations where semiconductor manufacturing — a mid-margin business — is not in direct competition with higher-margin and higher-profit activities like telecommunications, Internet companies and other hot businesses. While these higher costs may not concern semiconductor facilities that are geared toward making higher-margin products, it is a serious issue for commodity products such as memories and low-end foundry services.

However, the apparent cost penalties of a U.S. site can be mitigated when there are compelling business reasons for a facility based in the United States. Case in point: If a company has an existing infrastructure already in the United States, this can more profitably jump-start a greenfield facility in that location over a comparable site several thousand miles away. Likewise, the risks in U.S. sites are generally much better known and quantifiable compared with offshore sites, which makes it more likely that a program will meet budget and schedule.

Nevertheless, the inherent problems caused by the saturation of sites in the United States will mean that a majority of greenfield fab sites will, all other things being equal, go to lesser developed regions of Asia and Europe where costs are comparatively lower over the long haul.

### Lifecycle profitability

Site analysis and selection, from a company's perspective, should be concerned with only two major issues: profitability and business risks. However, the idea that fab sites can be quantitatively assessed with financial implications and detailed risk profiles is a relatively new concept for the industry.

Prior "state-of-the-art" techniques for assessment of sites involved using a static point-scoring model. Points were scored for each candidate site, identifying potential showstoppers and determining ways to work around them (with costs attached). This method included a crude discounted cash flow analysis for the project that does not quantitatively factor in critical issues such as project risk.

This assessment methodology, while capable of sorting out clearly "good" from clearly "bad" sites, does not fully account for the profitability and risk profiles for each site. For example, this methodology often totally ignores the severe profit penalty incurred when an engineering team is split in two to start up a heavily subsidized greenfield fab in a distant country. Such division of a company's human resources often means that the fab "losing" the crew takes a substantial dive in operational performance until such a time when the greenfield crew can stand on its own. Similarly, it is nearly impossible for a static point-scoring model to predict the substantial differences in facility productivity and ramp-up times at different sites or to make mid-course adjustments as project needs change.

Table 1 is from a previous article that presented a set of tools and techniques for guiding site analysis, selection and development process using Factory Commander as the "engine" for financial assessments.<sup>[2]</sup> This analysis accounted for the unique nature of the product being proposed for a facility, and the profit opportunity that such a product may face in the marketplace.

Facility	Firm A	Firm B	Firm C
Announcement	May 1996	August 1995	May 1995
Groundbreaking	October 1996	November 1995	December 1995
Completion	October 1997	December 1996	June 1997
Construction	11 Months	13 Months	18 Months
First tool install	October 1997	January 1997	Not Available

### Table 1. Facility Implementation Times

We began by recognizing that different products have different needs. A facility that manufactures DRAMs, which tend to have sharp spikes of profits followed by long periods of small profits or severe losses, has quantitatively different site and facility needs than a DSP facility with a more, consistent profit-ability profile. Assuming all three facilities in Table 1 have the same cost, Figure 3 illustrates the impact of delay on profitability. The delay is additional time in the construction phase relative to Firm A (best case).



Figure 3. The impact of delay on profitability, assuming all three facilities in Table 1 have the same cost.

Table 2 shows the break-even results from the Factory Commander cost model. This basic model also allowed us to estimate the profitability impact of a greenfield semiconductor program on a company's productivity at existing fabs. Starting a fab 500 miles away can have a steeply lower cost structure than starting a fab 5000 miles away.

Table 2. Break-Even Time Frame

Facility	Firm A	Firm B	Firm C
Delay	0 Months	2 Months	7 Months
Break-even	62 Weeks	69 Weeks	81 Weeks

Moreover, we are able to show that substantial productivity differences can be readily explained by site factors. For example, one foundry company found that its facility, located in what appeared to be a lower-cost location 45 minutes across the river from a cluster of fabs, experienced serious productivity problems caused by high rates of employee turnover. Turnover was strongly related to the distance between the fab and the location where the employees wanted to live. These long-term productivity losses eliminated the lower costs of the site. Our simulation readily identified these potential issues.

Since the 1998 article, we added further analysis to account for the risk profile of different greenfield sites. These include systematic ways of quantifying business interruption risks from such natural hazards as ice storms. The latest analysis methods allow us to craft programs that are inherently win-win. They help the manufacturer optimize for net profitability of a particular site adjusted for incentives, and help the governments and communities involved craft a mutually beneficial deal with a minimum of politically sensitive incentives. Because business conditions in this industry tend to change quickly, often what appears to be a good deal needs to be adjusted as conditions change. By being able to make such dynamic adjustments and show their financial and risk impacts quickly, we are able to better keep deals "on track" over the long haul.

### Summary

Semiconductor manufacturing is inherently a cyclical industry that faces periodic bouts of boom and bust on the way to the average 16% annual growth rate. Normally, it takes a process of years for a company to gradually pre-qualify and build the necessary infrastructure for greenfield fab sites by working with the community and governments involved. However, because of the severe slump in 1996-1998, the industry has cut back investments in this process worldwide even as we are about to hit a capacity "wall" that can only be met by quality 300 mm greenfield sites.

As the cost of 300 mm fabs continues to rise and the risk of failure becomes more and more unacceptable to industry, it is critical that an inventory of 300 mm qualified sites be available. Such sites will only be available if the industry can craft "win-win" propositions that sustain the industry, government and community partners involved when the industry encounters temporary setbacks. At the very heart of crafting "win-win" deals is the need for the partners to know precisely and quantitatively what is at stake for them financially and what risks are involved up front. Knowing what is at stake allows the partners to undertake appropriate programs to ensure the project's financial viability and to mitigate risks.

By using a set of software tools and techniques developed by the authors, we have been able to reduce the amount of time it takes to bring a qualified greenfield site on stream from a multi-year process to something that can be done in a matter of months. After such a site is qualified and selected, our tools allow the parties involved to make mutually beneficial mid-course corrections to keep the program viable over the long term as circumstances change. Tools and techniques, however, cannot make up for a basic ingredient of a successful program: the shared commitment to build a successful and profitable industry by industry, government and the community involved.

### References

- [1] Strategic Marketing Associates, in "Economic Indicator," Semiconductor International, Dec. 1999.
- [2] J. Kanz and D. Lam, "Wafer Fab Profit Opportunities and Costs," Semiconductor International, July 1998.



### Cost Impacts of Accelerated Ramp-up in 300 mm Logic Semiconductor Production Facilities

by Daren Dance and David Lauben, Wright Williams & Kelly

### Introduction

WWK has undertaken a study to estimate the impacts of accelerated ramp-up for a new semiconductor factory. In our study, we compare two possible production ramp conditions: a normal 12-month ramp and an accelerated 6-month strategy (fast ramp). We used a 6-metal layer copper process, equivalent in complexity to state-of-the-art logic and MPU chips, and assumed 300mm wafers as the product size. Throughput benefits from automation, though likely to reduce cost by reducing process load/unload times, were not considered in the analysis. This analysis was performed using WWK's Factory Commander™, a static cost and resource analysis model. The overall results from this analysis are summarized in Table 1.

Table 1: Cost Simulation Results			
Wafer Size	300 mm		
Number of Die/Wafer	375 <sup>1</sup>		
ASP / Wafer <sup>2</sup>	\$22,500		
ASP / Die	\$60.00		
Fast Ramp Benefits			
Year 1 Revenue	+ \$1,597 Million		
Year 1 Production	+ 79,850 Wafers		
Year 1 Cost / Wafer	- \$1,142 per Wafer		

Assumptions for this analysis are summarized in Table 2.

Table 2: Modeling Assumptions					
Factor	Value	Comments			
Starting Wafer Cost	\$600				
Wafer Processing Rate	20,000/mo	Full production after ramp up			
Processing Tools	155	51 different tool types			
Process Equipment	\$502.4 mil <sup>3</sup>				
Test Equipment	\$4.7 mil	Parametric and functional			
Measurement and Inspect Equipment	\$114.7 mil	Assumes 100% inspection <sup>4</sup>			
Cleanroom Cost	\$215 mil	Does not include office and support building requirements			
	\$3,700 / sq ft				
Operating Labor	409	Direct labor only			
Process Steps	410	Includes inspection and test			
Process Yield	100%				

We assume that expenditures for the cleanroom capital occur 12 months before start of production and the process, test, measurement and inspection tools expenditures occur 6 months before start of production<sup>5</sup>.

<sup>4</sup> 100% inspection is normal for initial stages of a production ramp. Inspection sampling plans can be introduced after the product and process have been characterized. Measurement and Inspection equipment released from production by use of sample plans is dedicated to yield and process improvement.

<sup>&</sup>lt;sup>1</sup> Based on 1999 International Technology Roadmap for Semiconductors Table 1a.

<sup>&</sup>lt;sup>2</sup> At start of production ramp

<sup>&</sup>lt;sup>3</sup> Thus the average cost per process system is \$3.2 Million for the logic process

<sup>&</sup>lt;sup>5</sup> Current production equipment backlogs range from 6 to 18 months. Thus the use of 6 months is conservative.

#### Impacts of Delay

Delays in reaching full production can be modeled by considering lost revenue and increased costs associated with longer time-to-volume. Some delays that can impact the start of full production include:

- Data analysis errors that require repeating production qualification lots, "engineers at International SEMATECH... found that 5% - 20% of messages transferred from tools to host systems were inaccurate."<sup>6</sup>
- Inaccurate process recipe downloads the require repeating production qualification lots.
- Equipment downtime due to software errors, "50% of tool downtime problems are caused by software."<sup>7</sup>
- Process delays due to wait for analysis results of send-ahead test wafers.
- Process delays lengthen process cycle time thus extending the learning curve.<sup>8</sup>
- Longer process cycles delay product introduction. Moore's Law estimates an ASP decline of about 2% to 2.5% per month for leading-edge products.<sup>9</sup>

The major driver for cost impacts of a delay in production is reduced output. Another driver is the continual decline of average selling price (ASP). The initial ASP of \$22,500 per 300mm wafer assumes no yield losses. Since Moore's law predicts an increase in functionality of 25% to 30% per year, we have represented the resulting ASP decline as a smooth 2% per month reduction based on the previous month's ASP. See Figure 1.

Figure 1 compares two initial ramp schemes that were modeled to estimate the impacts of production, including the factors listed in the previous section. Both ramp plans start at a nominal rate of 250 wafers per week. This is about 20 half lots<sup>10</sup>. The normal wafer processing cycle for a process of this complexity is about 4 to 6 weeks long. Under ideal conditions (Fast Ramp) after an integrated process is validated by 2 to 4 weeks of output, the start rate is doubled at 4-week intervals to identify and correct operational problems. Full production of 5,000 wafers (200 lots) per week commences after 4 weeks of production at 1,000 and 2,000 wafer per week start rates.

A more normal ramp rate requires 2 full production cycles (3 months) at 250 wafers per week before gradually increasing the production rate. Resolving operations, integration, and automation problems may require 4 to 8 weeks of debugging at each processing rate until production is gradually increased to 5,000 wafers per week 12 months after initial production.

<sup>&</sup>lt;sup>6</sup> Michael Chase, Douglas Scott, and Jeff Nestel-Pratt, "The challenges of macro integration for fully automated 300mm fabs," *Solid State Technology*, October 2000, p.53.

<sup>&</sup>lt;sup>7</sup> Dick Deininger, AMD, Strategic Business Conference, April 2000.

<sup>&</sup>lt;sup>8</sup> Elizabeth Campbell, Robert Wright, Joshua Cheatham, Mathias Schulz, and James Berry, "Simulation Modeling for 300mm Semiconductor Factories," Solid State Technology, October 2000, p.96.

<sup>&</sup>lt;sup>9</sup> This translates to 24% to 30% percent lower ASP per year which is consistent with assumptions in the International Technology Roadmap for Semiconductors (ITRS).

<sup>&</sup>lt;sup>10</sup> Each wafer carrier (FOUP) holds 25 wafers.





Figure 1: Production Rates and ASP by Month

### **Modeling Results**

Table 3 compares the logic process Factory Commander<sup>™</sup> modeling results for the 2 ramp up scenarios.

Table 3: Model Comparison						
	Fast Ramp	Normal Ramp	Benefit			
Capital Expenditure	\$837 million	\$837 million				
Year 1 Revenue	\$3,172 million	\$1,575 million	\$1,597 million additional			
Year 2 Revenue	\$4,323 million	\$4,323 million				
Year 1 Production	163,800	82,950	79,850 more wafers			
Cost per Wafer	\$2,784	\$3,926	\$1,142 Year 1 savings			

Rob Leachman, University of California at Berkeley, has estimated that a 1- day delay in time to market for a 200mm fab equals a loss of \$3.44 per wafer<sup>11</sup>. In comparing the two ramp scenarios, we estimate a loss of \$2.69 for each day lost in time to market over a 5-year product life. While Leachman's model and Factory Commander<sup>TM</sup> differ in many details, both models assume 100% yield and the same revenue per square centimeter. Thus we feel that our analysis is reasonable, if not somewhat conservative.

Figure 2 shows the additional net revenue from the Fast Ramp strategy as a function of wafer revenue. This will very for each company and depends on product mix. Note that even in the case of very low revenue per wafer, causing a net loss, the fast ramp strategy lowers the impact of the loss.

<sup>&</sup>lt;sup>11</sup> James A. Irwin, "The reasonably good status of 300mm wafer-processing tools," Solid State Technology, Oct, 2000, p. 90.



Figure 2: Sensitivity to Revenue per Wafer

### Conclusions

Based on an initial ASP per wafer of \$22,500 and including the impacts of Moore's Law<sup>12</sup>, we estimate that the 5-year average ASP per wafer for the fast ramp is \$13,505. The 5-year average ASP per wafer for the normal ramp is \$13,021, nearly \$500 per wafer lower. This difference is driven by the following factors:

- Higher production in the first year
- Higher OEE and utilization
- Earlier product introduction and higher initial ASP
- Higher throughput lowers equipment and labor costs

Thus the fast ramp could allow as much as \$319 million per year of additional revenue before yield loss. Although this analysis has not considered yield losses, based on historical analysis of revenue per fab, we forecast a more realistic revenue addition of \$150 million per year from the fast ramp, if normal production yields are included.

<sup>12</sup> ASP loss = 24% per year

### **TWO COOL®** v2.5 for Assembly & Packaging Released

Wright Williams & Kelly (WWK) has announced the release of its latest version of its flagship cost of ownership (COO) and overall equipment efficency (OEE) software, TWO COOL® for Assembly & Packaging. Enhancements included in this software release include: learning curve anlaysis of materials and consumables, conformance to SEMI E79-0200 (OEE standard), expanded sensitivity curve outputs, report on two column model column deltas, and database history tracking. This release is available at no charge to customers covered by warranty and maintenance agreements.