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Inside

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Factors in Determining COO for 300mm FOUPs

By Tracy Niebeling, Entegris

Overview

When analyzing 300mm FOUP costs, new fabs must go well beyond the initial purchase price. They must also consider various factors in carrier lifetime, utilization, maintenance, and spare parts in cost of ownership calculations. The various FOUPs available today are manufactured to different designs, from different materials, and for different levels of performance. All of these factor into the cost of maintaining and operating a given FOUP over its lifetime.

300mm fabs are being planned and built with an unprecedented degree of automation. Wafer carriers for 300mm —front opening unified pods or FOUPs —are no longer inert pieces of plastic. They are small machines that must operate with each and every process tool in a 300mm fab.

FOUPs have a much greater ability to reduce or increase the cost of chipmaking. They are expected to have a high level of performance, something that is reflected in their high purchase price. Any comparison of competing FOUPs needs to consider their operating costs over the life of a fab.

Basic COO model

The general model for cost of ownership (COO) is [1]

$$COO = (F\$ + R\$ + Y\$)/ (L \times T \times Y \times U)$$

Continued on page 3

Note: this is your last paper-based version of *Applied Co$t Modeling*. Future issues will be available on our website. See page 8.

Editorial Board

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Wright Williams & Kelly
39 California Avenue
Suite 203
Pleasanton, CA 94566

Phone 925-485-5711
Fax 925-485-3791
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2002 Calendar of Events

March

6-8 Beyond Budgeting Roundtable
Program Launch
Denver, Colorado
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July

17-19 SEMICON West 2002
Focus: Final Mfg.
San Jose, California

19-20 SEMI-sponsored seminar
"How To Successfully Manage New Product Introductions"
San Francisco Marriott
San Francisco, California

22-24 SEMICON West 2002
Focus: Wafer Processing
San Francisco, California
Visit WWK at Booth 6082

24 SEMI sponsored seminar
"Understanding and Using Cost of Ownership"
San Francisco Marriott
San Francisco, California

October

15-16 SEMICON Southwest 2002
Austin, Texas
Visit WWK at Booth 2205

where

F$ = fixed costs,
R$ = recurring costs,
Y$ = yield costs,
L = tool life,
T = throughput,
Y = composite yield, and
U = utilization.

Fixed costs are those that occur once during a tool purchase, such as purchase price, installation, training, and qualification. Recurring costs come up periodically during the life of a tool and include materials; consumables; utilities used for tool operation; periodic maintenance, repair and spare parts; and labor associated with all these activities. Utilization is a measure of time the tool is available for use, compared to the time the fab is in operation. Yield costs are a measure of damaged or defective die caused by a process tool.

Proposed FOUP COO model

I propose that the general model should be modified to calculate FOUP COO. A FOUP is similar to a process tool in that it performs a critical wafer processing function, but a FOUP is very dissimilar to a process tool in that there are many more FOUPs in a given fab, and a FOUP does not perform a process on the wafers other than providing them with isolation and safe transportation.

Below, I first consider the yearly COO of a single FOUP that is one of a large fleet of FOUPs necessary to run a fab. Then I simplify my FOUP COO calculation and make a proposal for COO factors for fixed and recurring costs, and the more indirect factors of utilization, throughput, and yield. Each of these factors has a unique flavor when applied to a FOUP, rather than a process tool.

A FOUP COO model could be [2]:

$$YCO = FPP/(LT \times U) + MC + SP + \Delta Y/N + \Delta T/N$$

where

YCO = yearly FOUP COO,
FPP = FOUP purchase price,
LT = lifetime of FOUP in years,
U = FOUP utilization,
MC = yearly maintenance cost/FOUP,
SP = yearly spare parts cost/FOUP,
ΔY = yield loss attributed to the FOUP,
N = number of FOUPs in a fab, and
ΔT = total change in process tool cycle time due to FOUP.

The first part of this equation deals with two factors that have a direct impact on the purchase price — FOUP lifetime and in-fab FOUP utilization rate. The new model adds in maintenance costs and spare parts necessary on a yearly basis over the lifetime of the FOUP. Finally, it includes two factors of wafer yield loss and change in process-tool cycle time. A perfect FOUP will have no impact on either of the latter factors. In the real world, however, FOUP selection can play a significant role in both of these in a production fab.

FOUP COO factors

It is instructive to look at COO as a pyramid built up from blocks of cost over time (*see Figure 1, page 4*). The total COO of a FOUP is built on a foundation of the cost factors of utilization, process tool throughput, and wafer yield. These are large costs and the most difficult to identify and relate back to a COO model. The factors of FOUP lifetime, maintenance, and spare parts make up the second row of blocks, and the FOUP

purchase price is at the top of the pyramid, where it is the easiest to identify and relate to the COO model. The cost factor of a FOUP purchase price is the one factor that is an absolute. You need only look at a shipping invoice to determine the price and shipping costs per FOUP as delivered to a given fab. FOUP lifetime, FOUP maintenance costs, and the cost for spare parts over the life of a FOUP are more difficult to predict. The FOUP maker should be able to predict the service life of its product under "normal use."

Likewise, the costs of FOUP maintenance and associated spare parts should be easily estimated for "normal use." Each fab will probably have a slightly different result in the maintenance and spare parts areas, however, so estimates will need to be improved with time and experience. Cost factors for FOUP utilization, process equipment throughput, and wafer yield loss will be the most difficult to estimate, but these factors will probably prove to be of greatest value and will also present the greatest opportunity for improvement in FOUP COO.

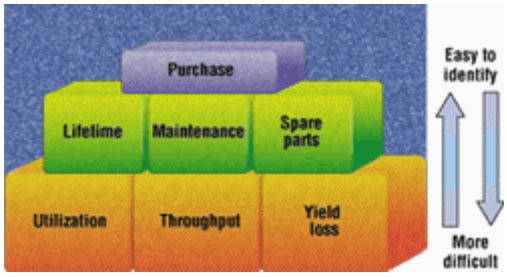


Figure 1. Building blocks for a comprehensive COO model [3]

Purchase price vs. lifetime, utilization

The most basic COO calculation divides the purchase price by the expected life of a product to yield a cost/unit time measure. Fundamentally, this is true for a FOUP. A FOUP that will last through five years of fab use will be a better value than a FOUP at the same price that lasts only two years. However, I further refine this simple metric by calculating utilization and using this fraction to discount the expected FOUP lifetime.

The purchase price of the FOUP is the easiest cost to determine. The general COO model recommends that we consider together all fixed costs of procurement and installation of a piece of process equipment. For a FOUP, the purchase price is the major fixed cost with installation costs being very minimal. In some cases, the shipping cost of a FOUP might also be significant so the costs of shipping, freight, taxes, and duty might also be added into the FOUP purchase price for COO calculations.

The lifetime of a FOUP is a prime COO consideration. A typical FOUP is designed for five years of service. This is typically tested by a marathon of door-open-and-close cycles. (International Sematech has suggested 161,000 open-close cycles assuming 10,000 cycles/year, a 2:1 safety factor, and a statistical allowance for testing of small number of samples.) Design, materials, and manufacturing workmanship will all factor into the lifetime of a FOUP, but useful FOUP lifetimes will not be known for sure until a population of FOUPs has been used in a production fab for many years.

A given FOUP will not always be available for the transport of a wafer lot. There will be time spent in washing and maintenance, as well as time spent repairing the inevitable damage due to mishaps in the fab. All of these things will keep the FOUP away from 100% utilization. The following is a formula that might be helpful in the estimation of FOUP utilization:

$$U = 1 - (SM + USM + A + S)/H$$

where

U = utilization or hours a FOUP is available to hold wafers, out of the total number of hours of fab operation,
SM = scheduled maintenance time (hrs/wk),
USM = unscheduled maintenance time (hrs/wk),
A = assist time (hrs/wk),
S = standby time (hrs/wk), and
H = total fab production hours scheduled per week.

Scheduled maintenance includes periodic washing and re-qualification for use, as well as periodic renewal of the breather filter, door seal, and any other part that will wear out during use. Unscheduled maintenance includes work necessary to repair and re-qualify any damaged FOUP. Assist and standby times are those periods before and after a scheduled or unscheduled maintenance during which the FOUP cannot be used for the transport of wafer lots.

All of these times should be estimated in hours/week and then, when factored into the total number of fab production hours scheduled each week, we can calculate the utilization factor for the FOUP. Actual utilization rates on FOUPs in a given fab will no doubt be highly dependent on a fab's practices. In some facilities, there will be a philosophy of running the FOUPs until they have an obvious failure. In other fabs, a strict preventive maintenance schedule will be followed to minimize failures. Hence, an accurate estimation of FOUP utilization might be very difficult to achieve.

Maintenance, repair, spare parts cost

I have already talked about using estimations of maintenance and repair times in the calculation of FOUP utilization. The next step is to estimate the actual costs of performing maintenance and repair, as well as the cost of the necessary spare parts. A FOUP manufacturer should be able to give a recommendation for washing frequency and the schedule for renewing the breather filters and door seals.

These schedules will be a function of FOUP use cycles, but should be easily converted to an estimated yearly cost. Likewise, estimation of the cost of spare breather filters, door seals and any other service component should be easy to estimate based on the supplier's price list. A key consideration will be to gauge how well a FOUP has been designed for maintainability. A FOUP with a low number of parts, and designed for easy disassembly and re-assembly will result in lower maintenance costs.

What will not be easy to estimate is the cost to repair FOUPs damaged during use in the fab. This reparable FOUP damage can be expected to be higher during the fab's early, ramp-up stage, and then to taper off as experience is gained, process tools dialed in, and AMHS installed and de-bugged. This expense should be expressed as a cost/year/FOUP. A key factor in repair costs will be how well the FOUP has been designed for repair. A simple and repair-friendly design will result in lower repair costs.

Process tool throughput

A major concern in any wafer fab is the throughput of the process tools. In a 300mm fab, wafers are delivered to each process tool in a FOUP by way of a standard load port. Wafer throughput in a given tool can hinge on the performance of the FOUP. The FOUP can influence process tool throughput in two general areas of wafer transfer and wafer cooling.

One of the main functions of a FOUP is to present the wafers in a predictable location. The measure of a FOUP's ability to hold the wafers is called wafer plane. A 300mm FOUP is required by Semi standards to hold each wafer in the correct position with a vertical tolerance of ±0.5mm. A FOUP population that has precise wafer plane performance in each FOUP and consistent wafer plane performance across all FOUPs will allow the quickest wafer transfer, for the greatest process tool throughput. This same FOUP population will also tend to minimize particle generation and wafer damage, as discussed later.

Another differentiating factor between front opening unified pods of different designs and materials of construction is their ability to accommodate hot wafers. Many wafer processes have a cool-down step at the end of the process. This cool-down is necessary to ensure that the wafers do not exceed temperature limitations of a FOUP. A front opening unified pod with higher temperature-capable materials, especially where wafers make contact, can allow a shortening of the cool-down time.

This can contribute to greater process tool throughput. For example, a FOUP with wafer supports constructed of a polyaryletheretherketone plastic, with a melting point of 340°C, will accept wafers coming from a hot process at 300°C. A FOUP with wafer supports made from polycarbonate, with a melting point of only 140°C will require much more wafer cool-down time, reducing process tool throughput.

To account for the effects of a FOUP in the area of process tool throughput, the following equation can be used:

$$\Delta T = \Delta T_t \times N_t \times R_t + \Delta T_c \times N_c \times R_c$$

where

ΔT = total change in process tool cycle time due to FOUP,
ΔT_x = change in time required for a process in hours due to FOUP,
N_x = number of times a process is performed per year,
R_x = cost/hr for process being performed (i.e., process equipment cost in $/hr),
t = wafer transfers, and
c = cooling of wafer after high-temperature process.

Wafer-yield costs

Yield is perhaps the most difficult COO factor. It is also very likely the greatest opportunity for cost savings for any FOUP. The reason that yield is a difficult factor is not that yield numbers are hard to calculate, it is just that yield numbers are always considered by wafer processors to be proprietary information. In addition, while yield is visible and easy to calculate, it is often impossible to attribute a given yield loss to a particular fab tool such as a FOUP.

FOUPs can contribute to wafer yield loss in the three modes: particle generation, molecular contamination, and wafer damage or breakage. Wafer breakage is usually caused by a catastrophic event such as an AMHS dropping a FOUP, a misaligned load port, or perhaps an out-of-spec wafer plane on a FOUP that is damaged but still in service. Wafer breakage is normally a random event and very hard to predict.

Molecular contamination is another area where FOUPs can contribute to wafer yield loss. The molecular contamination potential of a FOUP is commonly measured by an outgassing test. It is important that any outgassing testing be done with a complete FOUP assembly so as to include the molecular contamination potential of all components of the FOUP. Careful materials selection and control by the FOUP vendor are the only ways to minimize molecular contamination. In the determination of a contamination source, it is important to separate outgassing from the FOUP materials from molecular contaminants that are being transported from one process to another on the wafers or inside the FOUP. This type of cross contamination cannot be blamed only on the FOUP.

The final and most important yield loss contribution factor with FOUPs is their particle contribution to the wafers. A main function of the FOUP is to provide an isolated environment for the wafer lot, protecting wafers from particles that are circulating in the fab air. A well-designed FOUP will have an effective door seal so particles cannot enter a closed FOUP. It will also have a breather filter that allows air to enter the

FOUP for pressure equalization, at the same time excluding the particles in that air. Another source of particles in a FOUP are those that are generated by the opening and closing of the FOUP door, and those generated by the transfer of the wafers into and out of the FOUP. Careful selection of materials, good design, and precise wafer planes all contribute to a low-particle FOUP.

In the estimation of wafer yield loss attributed to FOUPs, the following equation will be helpful:

$$\Delta Y = (Y_p + Y_m) \times W_y \times D_w \times V_d + B \times D_w \times V_d$$

where

ΔY = total annual yield loss attributed to FOUPs,
Y_p = fractional yield loss due to particles coming from FOUP,
Y_m = fractional yield loss due to molecular contamination coming from FOUP,
W_y = wafer starts/yr,
D_w = die/wafer,
V_d = value of each die, and
B = number of broken wafers attributed to FOUPs/year.

Conclusion

I have proposed a simplified COO model for 300mm FOUPs and discussed the various cost factors that should be considered during a FOUP evaluation. This COO approach will allow for a rational comparison of various FOUPs based on what they will cost to operate in a wafer fab over the long haul, rather than just by the purchase price. The main cost factors in FOUP COO calculations should be purchase price, carrier lifetime, maintenance and spare parts cost, FOUP utilization and the effects of the FOUP on process tool throughput, and wafer yield. This is intended to be a basic treatment of COO. Each new wafer fab will have special requirements that will lead to the inclusion of more and different cost factors in the COO analysis.

References

1. Taken from seminar materials published by Wright, Williams and Kelly, Pleasanton, CA.

2. Adapted from K. Mikkelsen, "Transport and storage wafer carrier COO,"Proceedings of the Advanced Semiconductor Manufacturing Conference and Workshop, Cambridge, MA, 1995.

3. Adapted from D.L. Dance, D.W. Jimenez, "Applications of COO," Semiconductor International, Sept. 1994.

A Change in *Applied Co$t Modeling*

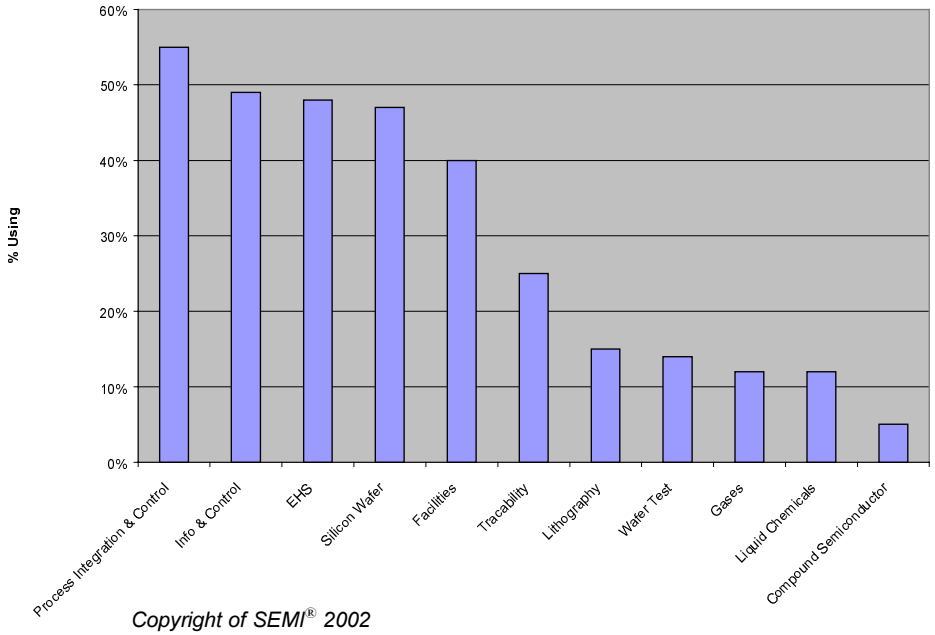
With the new year comes a change in how *Applied Co$t Modeling* will be distributed. Beginning with the next issue, March 2002, *Applied Co$t Modeling* will become an e-zine and will no longer be mailed. It will be accessible by visiting http://www.wwk.com and clicking on the "Newsletter" button. At this site you will find not only the current issue, but also previous issues.

We are providing this new format for ease of distribution and hope that you will enjoy reading each issue of the newsletter. It will continue to be published quarterly with the next issue produced in March. The newsletter will be in .pdf format and viewable and printable by using Adobe Acrobat Reader.

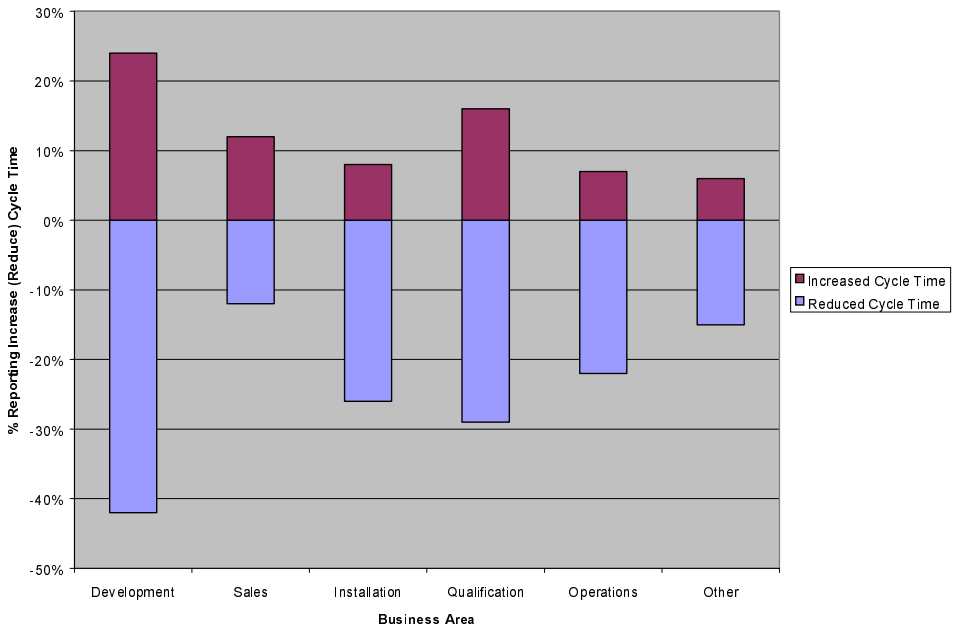
SEMI® Standards Survey

In an effort to better understand the impact of standards on 300mm developments, SEMI® conducted an industry survey during September 2001. The results show how 85 respondents perceive that 300mm standards are impacting their cost and cycle times.

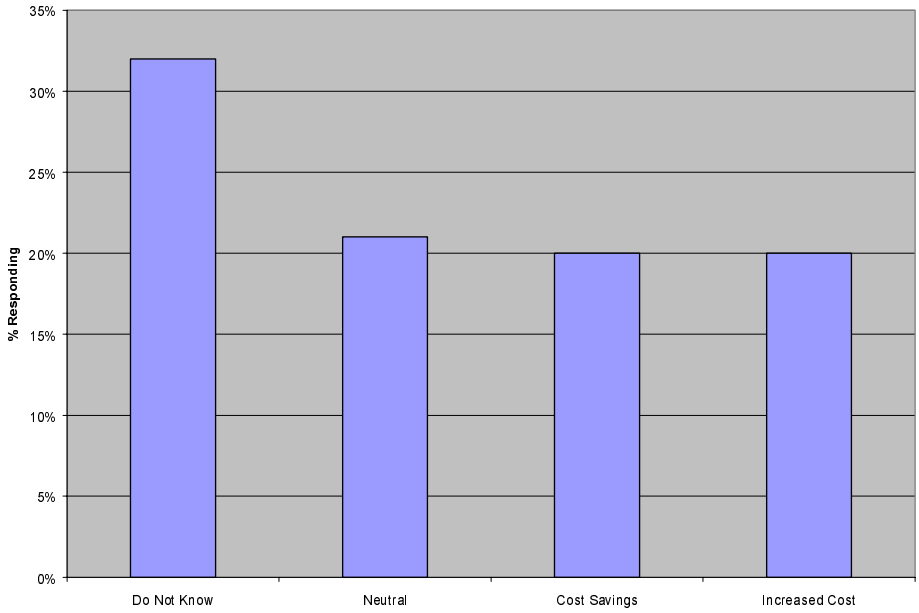
More than 85% of the respondents are using 300mm standards. The following chart shows the types of standards that are being used.



Over 60% report that the availability of 300mm standards has increased the use of standards for procurement over the last four years. In most cases, respondents feel that the use of 300mm standards is reducing their cycle times in the following areas.



While nearly half report that standards are being developed soon enough to reduce costs for 300mm, over a third disagree that development is soon enough. This is confirmed by the mixed response to the questions, "What was the financial impact of standards for 300mm on your company over the last four years?"



Challenge for the new millennium: Managing mask costs

Kenneth A. Rygler DuPont Photomasks Inc.

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There has been growing concern over the so-called million-dollar mask set. While the cost of producing advanced photomasks continues to increase, they remain the lowest-cost approach to staying on pace with Moore's Law. Though some say that the move deeper into the subwavelength era will see a sharp rise in mask costs, management strategies can mitigate these costs.

Application-specific integrated circuits (ASICs) power much of today's electronic equipment. Semiconductor manufacturers want to capitalize on their intellectual property (IP) through the development of unique products, many of which are ASICs. Non-recurring engineering (NRE) charges, which include the cost of masks, must be managed in a way to allow the continued proliferation of ASICs. Otherwise, chips will migrate from application-specific to standard to commodity products. The result is a production game more easily won by those with the lowest production costs and access to the most capital — not necessarily those with the best ideas.

While the cost of masks for standard products such as microprocessors and DRAMs can be amortized over long wafer runs, ASICs are usually produced in smaller wafer lots. Clearly, on the basis of number of runs/mask, ASICs become more expensive to produce as mask prices increase. But consider this: as a percentage of NRE costs, mask costs for ASICs may actually be the same or lower than they were five to 10 years ago. Feature sizes of 0.18µm and below allow a single system-on-a-chip (SOC) to have the same functionality as multiple chips found in older electronic systems. To the extent that many of these chips were ASICs, each of those individual chips required a mask set with its own NRE, as well as complex multilayer boards and other interconnects. If one compares the photomask costs and associated NRE charges for producing the same functionality in a single chip vs. multiple chips, today's more complex photomasks deliver far more bang for the buck than they did 10 years ago.

But beyond increased value per mask, there are strategies that can effectively reduce mask costs. A primary one is the growth in collaboration among chip designers, their EDA tool suppliers, and photomask manufacturers earlier in the image-creation process. Eliminated is the "trial and error" of mask design and the accompanying cost in time and materials. This will also help to ensure that designs are more photomask- and lithography-friendly and that they are more cost-effective to produce.

New strategies in prototyping and low-volume wafer runs can also reduce costs. For example, DuPont Photomasks is working with both integrated device manufacturers (IDMs) and foundry customers on multiproduct wafers, allowing several devices to be contained on a single reticle set. Other chipmakers are utilizing smaller fields for prototypes and low-volume runs, trading lower reticle costs for some reduction in stepper throughput. With the current low capacity utilization in many fabs, this may be an attractive route.

For photomask producers, inspection strategies that eliminate redundant inspections and focus on detecting and repairing only printable defects can reduce the cost of maskmaking. Accepting reticles with defects that have no effect on device performance or wafer yield is a cost saver, in time and money.

Overall, mask prices will come down from their introductory-level prices. At each technology node, prices tend to be very high, as tools designed for older photomask technology are extended to build prototypes. As volumes grow, however, yields improve and advanced tools and processes are introduced, and improved productivity and yields lead to price reductions. So while initial 0.13µm photomask sets may have approached $1 million, this price is expected to decline.

Other opportunities exist to reduce substantially the costs of producing subwavelength reticles. For example, we are creating special photomask sets for chipmakers in the high-wafer-volume, high-performance segment (e.g., DRAMS, microprocessors), medium-wafer volumes (SOC, FPGA, DSP, ASSP), and low-wafer volumes (ASIC). The key to these offerings is the degree to which we implement lower-cost, high-performance, laser-based processes as opposed to more expensive electron beam processes.

Optical lithography will continue to extend the semiconductor industry's capabilities beyond the limits we see today, as it provides the lowest-cost, lowest-risk path to achieving the semiconductor mantra of the last 50 years: smaller, faster, cheaper. To do this will require unprecedented cooperation between design, photomask, and lithography companies, which can also enable the small wafer volume applications to continue to thrive. 

Software Version Index

The following are the latest releases for WWK's software products. . .

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