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S-FIL™ Technology: Cost of Ownership Case Study

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Abstract

The escalating costs of lithography for the sub 90nm regime have been well documented. The semiconductor industry is exploring evolutionary improvements to existing photolithographic techniques as well as disruptive, but cost effective patterning technologies for the demanding high-resolution requirements.

Step and Flash Imprint Lithography (S-FIL™) is an innovative patterning technology commercialized by Molecular Imprints. S-FIL has demonstrated the capability to pattern very high-resolution features and has been recognized as an NGL candidate by inclusion on the ITRS Roadmap in December 2003. This paper describes the S-FIL process and examines its comparative cost of ownership relative to conventional photolithography at the 90nm node and to immersion photolithography at the 65nm node.

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Shanghai, China

April

12-14 **SEMICON Europa**
Munich, Germany

May

4-6 **SEMICON Singapore**
Singapore

9-11 **International Conference on Integrated Circuit Design and Technology**
Austin, TX

9-11 **Strategic Business Conference**
Welches, OR

15-18 **The ConFab**
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6-7 **International Strategic Symposium**
Osaka, Japan

8-10 **Flat Panel Display Taiwan**
Taipei, Taiwan

July

12-14 **SEMICON West**
San Francisco, CA

14 **Understanding and Using Cost of Ownership Workshop**
San Francisco, CA

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Introduction

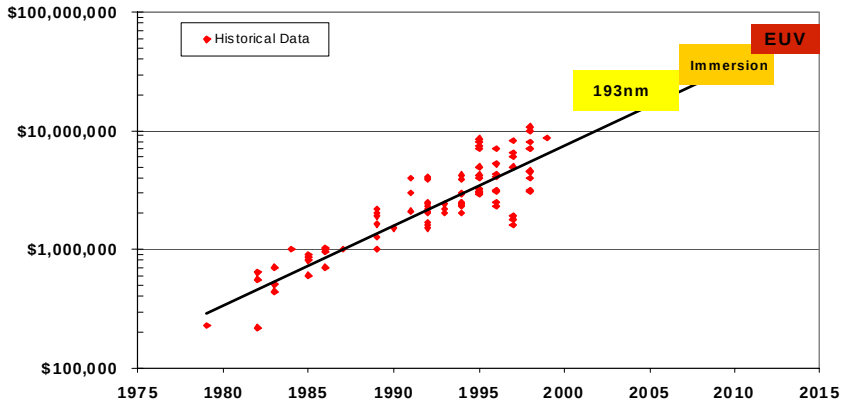
Historically, the lithography technology of choice has been photolithography. The minimum feature size (F) in photolithography is given by: $F = (k1)(\lambda)/NA$. Here λ is the exposure wavelength, NA is the numerical aperture of the lens system in the photolithography tool with typical values of 0.5 to 0.8, and k1 is a process related term with typical values of 0.4 to 0.7. The reduction of F has been achieved by periodically going to smaller and smaller exposure wavelengths. Photolithography has been operating at a deep UV wavelength of λ = 248 nm, while λ = 193 nm has been in production more recently and the near future appears to welcome 193nm immersion photolithography which has been in beta testing [1].

Until a few years ago λ = 157 nm was being investigated along with extreme ultraviolet lithography (EUV), which operates at λ = 13.2 nm. This continuous reduction in wavelength combined with highly sophisticated designs of lenses and mirrors, design of advanced and complex masks, innovation in materials, processes, and precision machines has enabled sub-100nm lithography. However, with shorter wavelengths, there are long lists of new and substantial technical challenges. For instance, fused silica has been the established lens material in optical lithography. But, fused silica is not transparent at 157 nm. Therefore, the 157 nm research efforts were focused on using CaF_2 as the lens material, which led to significant original research problems with respect to manufacturing sufficient quantities of high-purity CaF_2 and circumventing the high level of birefringence that is characteristic of this material. At λ = 13.2 nm, there are no known transparent materials; therefore, all the optical systems and photo masks are based on reflective optics. Further, obtaining a source with sufficient power at this EUV wavelength is still an open problem. High-resolution e-beam lithography techniques, though very precise, are too slow for high-volume commercial applications. They are believed to be best suited for directly writing photo masks used in photolithography.

In the interim, 193nm immersion photolithography has emerged as a very high potential technology contender at the 65 nm node. In immersion lithography, a liquid is interposed between an exposure tool's projection lens and the wafer. Immersion technology offers the opportunity for better resolution over conventional projection lithography because the lens can be designed with NAs greater than one, thus creating the ability to produce smaller features.

The Exponential Cost of Going Smaller

It is not physical limits, but prohibitive costs that are likely to make the traditional photolithography approach of decreased wavelength impractical. Even today, optical lithography is an extremely expensive unit process. Historically, the purchase price of optical exposure tools has increased exponentially (see Figure 1 below). Even if



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fundamental challenges are overcome at λ = 157 nm and 13.2 nm, it is believed that the historical exponential increase in tool cost could become even steeper.

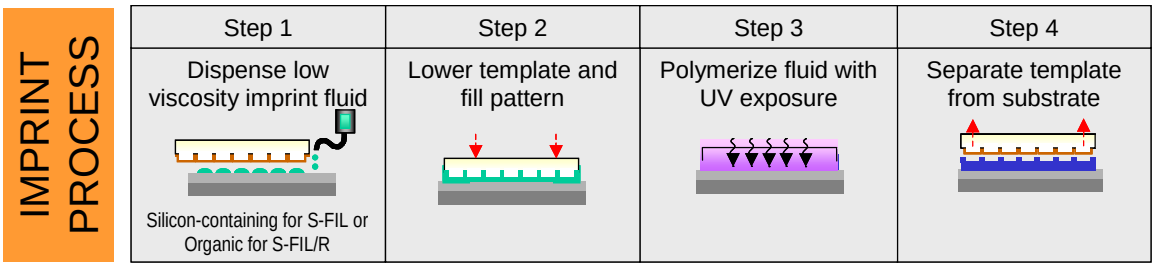
Preliminary list price estimates for a EUV prototype/alpha tool expected to be ready by 2007 are $ 47 M with a throughput of 10 WPH [2]. In addition to the cost of the tool, the recurring and consumable costs associated with process materials, environmental control, complicated photomasks, etc. makes next generation lithography a high-risk proposition.

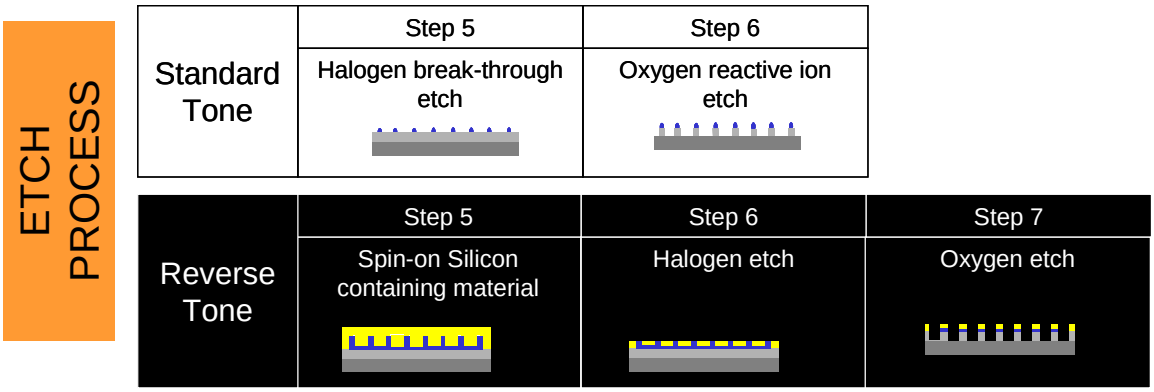
The only way to recover these costs is to have high throughputs and/or long tool lives and/or long photomask lives, and excellent feature fidelity within a field, between fields, and between wafers. While lithography was primarily developed by the silicon microelectronics industry, it is fast becoming a key unit process for other application areas such as micro-fluidic devices, optical switches, flat panel displays, and SAW devices. Emerging nano-resolution applications include sub-wavelength optical components, biochemical analysis devices, high speed compound semiconductor devices, distributed feedback lasers, photonic crystals, and high density patterned magnetic media for data storage. The above discussion clearly indicates that there exists a need for low-cost alternatives to nano-resolution photolithography. It is believed that if a sufficiently low cost lithography solution can be developed, it will provide a major competitive edge to manufacturers of traditional and emerging devices, and enable new kinds of devices that are currently not economical. The cost and complexity trends in photolithography have motivated Molecular Imprints, Inc. to investigate and develop a non-optical, low-cost lithography technique known as Step and Flash Imprint Lithography (S-FIL).

The S-FIL™ Technology

S-FIL technology was developed by a team supervised by Professors S.V. Sreenivasan and Grant C. Willson of the University of Texas at Austin. Molecular Imprints Inc. has exclusively licensed this technology from the University of Texas at Austin, and subsequently improved upon it. The process includes the use of a proprietary imprint fluid that serves the role of a resist in the S-FIL process. The S-FIL process has been well documented [3]. S-FIL involves imprinting sub-100 nm sized features on to a pre-planarized substrate using a template (mold). The template is usually manufactured from an industry standard mask blank made of fused silica using a phase mask process. The main difference being that the feature sizes on the template are 1:1 rather than 4:1.

Enhancements to the S-FIL process resulted in a new process called S-FIL/R™. The S-FIL/R process was described in [4]. The following figure illustrates the S-FIL/R process:





The S-FIL/R process enables good critical dimension control on wafers with moderate levels of topology. The transfer etching process is straightforward and does not involve any unusual gases or etch techniques. The advantages that S-FIL/R provides over S-FIL include the following i) Improved line-width control with no faceting at the line edges, ii) Improved critical dimension control over topography iii) Formation of "T"-topped features suitable for lift-off processing and (iv) Improved etch resistance and selectivity during pattern transfer.

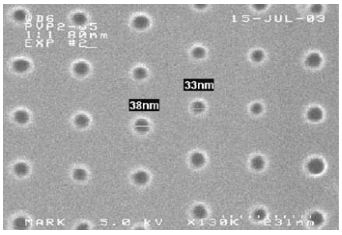
For the purposes of this paper, we have considered S-FIL/R process as the baseline process.

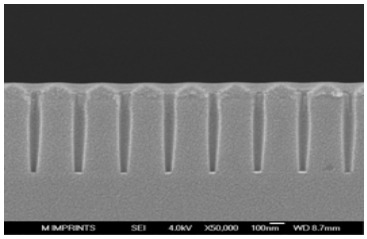
Cost of Ownership Analysis

Molecular Imprints has teamed up with Wright Williams & Kelly, Inc. (WWK), well known in the semiconductor industry for their industry standard software tools and expertise in calculation of cost of ownership. WWK's TWO COOL® software tool is used by OEMs, chip manufacturers, and others to develop a comprehensive cost of ownership model of semiconductor tools and processes.

S-FIL/R, despite being a new entrant in the field of semiconductor lithography, has generated strong interest. In 2003, the ITRS included imprint lithography on the roadmap [5]. Although this roadmap currently applies imprint lithography to the 32 nm node and beyond, Molecular Imprints believes that imprint technology offers possibilities in the immediate future.

One of the key demonstrated capabilities of imprint lithography has been the ability to imprint sub-100 nm contacts. Figure 3 below demonstrates results obtained by Molecular imprint using its Imprio™ 100 imprint lithography product.





Another interesting ability of imprint technology is to be able to imprint 3-dimensional features such as the one shown below in Figure 4. The imprint shown below was obtained using a 3-tier template. This capability raises the possibility of imprinting a via-trench combination (2-tier template) in dual damascene patterning processes in a single step as opposed to 2 masks needed in photolithography. Fig 5 illustrates actual dual damascene process results using a 2-tier template.

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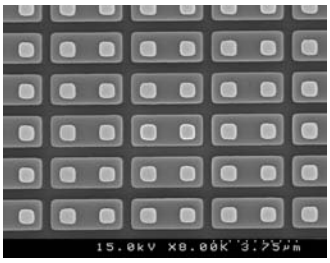
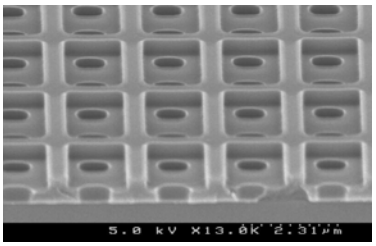
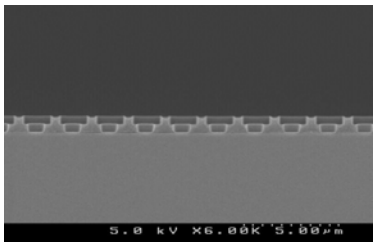






The above two examples are considered in this paper to demonstrate the attractiveness of imprint technology from a cost of ownership perspective.

S-FIL vs. Conventional Photolithography at the 90nm node

The following assumptions were utilized for the cost of ownership study. Note the values assumed for the imprint process are based on logical extensions of the current state of imprint technology offered by Molecular Imprints. In order to critically examine imprint technology, a sensitivity analysis is conducted around key imprint lithography parameters such as tool throughput, template usage and template price. This sensitivity analysis is presented in the sections following the cost of ownership results.

Parameter	**Photolithography**	**S-FIL/R**
Tool Price ($)	20 M[1]	10 M
Installation Cost ($)[2]	1 M	0.5 M
Mask/Template Price ($)	**62,500**	**25,000**
Effective Throughput (WPH)	60	50
Mask/Template Usage	2000 wafers	2000 wafers
Wafer Size	300 mm	

A key difference in the costs of the two technologies is the difference in the template/mask Pattern generation cost for template is lower than for a conventional photo mask because the templates need no optical proximity correction. Pattern writing times (a key cost driver for masks) is 4-times shorter because of smaller field sizes ($1/16^{th}$ the area of traditional photo masks). Again templates need shorter pattern writing times because of smaller data-preparation files (no optical proximity correction factors (OPC) etc.). Again the template inspection is over a smaller area and hence lowers the cost.

For conventional photo masks, even though they have an advantage of 4:1 reduction ratio, the write times are not short because the feature sizes of MEEF, OPC, etc are approximately 1.5 the actual feature size. Based on all of the above, initial cost estimates show that templates are lower cost than photo masks.

[1] Does not include resist coating/baking/developing equipment
[2] Installation Cost is estimated at 5% of equipment purchase costs. Transportation costs have not been included

Contacts at the 90 nm Node

The first cost of ownership analysis investigates patterning of the metal layer 1 (M1) for a 4-layer DRAM device. Per the ITRS specifications, this layer is the most demanding in terms of the pitch. Photolithography techniques struggle with the pitch specifications even at today's 90 nm node levels. Memory device designers have to adhere to numerous design rules to avoid the so-called "forbidden pitch" ranges.

The main drivers of the cost of ownership, as revealed by the output from TWO COOL® software, are displayed in Table II below.

COO Driver	Photolithography	S-FIL/R	% Difference (Relative to S-FIL/R)
Mask & Materials	$35.83	$14.67	59%
Equipment Depreciation	6.72	4.03	40%
Maintenance[3]	0.21	0.26	-24%
Labor	0.20	0.24	-20%
Total COO per wafer[4]	**$43.10**	**$19.37**	**55%**
COO (5,000 wafers/wk)	$44.96	$21.28	53%

It is clear that the mask & materials costs and the equipment depreciation are the principal cost components of each technology. They are also the clear differentiators between S-FIL/R and photolithography. The above analysis shows a 55 % reduction in cost using imprint lithography as opposed to photolithography.

A key advantage of imprint technology is its elimination of the "forbidden pitch" rule. Imprint lithography allows relaxation of some of the 2,000 additional design rules that must be implemented for reticle enhancement techniques and optical proximity correction that allow optical lithography to meet technology requirements [7]. These design rules add complexity, which in turn, add time and cost to chip designs and increase the probability of manufacturing problems. The design rules also increase the physical size of the chip, which leads to fewer die per wafer, lower yield and higher cost per chip.
As an example, design rules that increase the die area 15% from 140 mm^2 to 150 mm^2 reduce the gross die per wafer by 7%, lower yield by 0.8%, and increase die cost by 8%.

Dual Damascene Process at the 90 nm Node

As discussed above, S-FIL/R raises some very exciting possibilities for cost savings in the dual damascene process. By using a 2-tier template, S-FIL/R can imprint via and trench in a single lithography step. This provides a dual advantage in process cost and template cost. A cost of ownership analysis for dual damascene was conducted using TWO COOL® from WWK.

Except for the template cost, all assumptions remain the same as in Table I.

[3] Assumes same Maintenance and Labor costs for each type of system
[4] At 100% utilization

Parameter	Photolithography	S-FIL/R
Tool Price ($)	20 M[5]	10 M
Installation Cost ($)[6]	1 M	0.5 M
Mask/Template Price ($)	**62,500 (1 for via and 1 for trench)**	**75,000 (2-tier template)**
Effective Throughput (WPH)	60	50
Mask/Template Usage	2000 wafers	2000 wafers
Wafer Size	300 mm	

A COO analysis for just the lithography steps using the TWO COOL software validates the significant cost advantage of the S-FIL/R for the dual damascene process over conventional photolithography. Nearly 50% reduction in cost is observed for the lithography steps as shown in Table IV below.

Photolithography		S-FIL/R	
Masking Step	COO	Imprint Step	COO
Metal Mask	$43.10	Metal/Via Imprint	$47.58
Via Mask	$43.10	--	--
Total Masking Costs	$86.20	Total Imprint Cost	$47.58

While the above analysis considers only the litho steps, it is essential to look at the impact of integrating imprint lithography into the complete dual damascene process. To compare process costs, WWK's Factory Commander® was used to examine the Metal 1/Metal 2/Via 2 sequence for 5,000 wafers per week from an example process. Developed with Sandia National Laboratories, Factory Commander® is a Cost and Resource Evaluation software platform that can be applied to any discrete manufacturing or assembly operation. It performs high-level cost analyses of overall factory and individual product costs, manufacturing capacity, and revenues. Note, all measurement and inspection steps have been excluded in this comparison between photolithography and S-FIL, but building depreciation has been included, which was excluded in the previous TWO COOL® COO examples. Table V compares processes and Table VI compares COO cost drivers.

WWK Offers Free Windows Desktop Wallpaper

Wright Williams & Kelly (WWK), a cost & productivity management software and consulting services company, announced today the availability of free Windows Desktop Wallpaper on its web site (www.wwk.com) under their "Resources" link. The wallpaper selections are based on the company's award winning graphics, including the TWO COOL® flying "Borg" cube.

"Over the years WWK has developed a large portfolio of interesting graphic designs," stated David W. Jimenez, WWK's President. "Many of these images have been used internally and we thought it was appropriate to find a vehicle to share them with our clients and anyone else interested in creating a unique computer desktop experience. We hope people enjoy the images as much as we enjoyed working with The Wecker Group of Monterey, CA (www.weckergroup.com) to create them."

[5] Does not include resist coating/baking/developing equipment
[6] Installation Cost is estimated at 5% of equipment purchase costs. Transportation costs have not been included

Photolithography Process	COO	S-FIL/R Process	COO	Comments
Deposit ILD	$9.29	Deposit ILD	$10.62	
		BARC	3.70	Photolithography may not require BARC
Backside Clean	3.50	Backside Clean	3.63	
Metal 1 Mask	51.16	Metal 1 Imprint	31.99	Includes resist coat and develop
		Spin Silicon	8.27	S-FIL/R specific process step
Etch Channel	4.21	Etch Channel	4.48	
Ash	1.48	Ash	2.16	
Barrier/Liner/Seed	20.53	Barrier/Liner/Seed	21.57	
Cu Deposit	4.68	Cu Deposit	4.91	
CMP	11.26	CMP	11.66	
Post CMP Clean	2.23	Post CMP Clean	2.35	
Low K Dielectric Deposit	9.29	Low K Dielectric Deposit	10.62	
Etch Stop	20.53			
ILD	9.29	BARC	3.70	Photolithography process may require BARC (not shown)
Backside Clean	3.50	Backside Clean	3.63	
Metal 2 Mask	51.16	Metal 2 Imprint	51.74	S-FIL/R uses 2-Tier template
		Spin Silicon	8.27	S-FIL/R specific process step
Etch Channel	4.21	Etch Channel	4.48	
Ash	1.48	Ash	2.16	
Backside Clean	3.50	Backside Clean	3.63	
Via 2 Mask	51.16			Photolithography process step
Etch Nitride	8.76			
Etch Via	5.97	Etch	9.30	
Ash	1.48			
Backside Clean	3.50			
Barrier/Liner/Seed	20.53	Barrier/Liner/Seed	21.57	
Cu Deposit	4.68	Cu Deposit	4.91	
CMP Cu	11.26	CMP Cu	11.66	

Driver	Photolithography	S-FIL/R	% Difference
Mask & Materials	$127.33	$83.63	34%
Equipment Depreciation	117.49	94.70	19%
Building Depreciation	47.27	47.23	0%
Maintenance	22.18	12.12	45%
Labor	4.38	3.33	24%
COO (5,000 wafers/wk)	**$318.64**	**$241.02**	**24%**

For the 90 nm node dual damascene process, due to the reduced difference between the costs of the template and photo mask for the, the impact on COO of S-FIL/R is diluted but still delivers a significant improvement of 24%.

S-FIL/R vs. 193nm Immersion Photolithography at the 65nm node

S-FIL/R offers a larger COO advantage at the 65nm node than at the 90nm node because template price is less sensitive to changes in the feature sizes for the contacts/via/trench. Again as explained earlier, because the S-FIL/R templates do not require any optical proximity corrections (OPC's), since the S-FIL/R process exactly replicates the templates. On the other hand, photo masks do need OPCs and other correction factors that significantly increase the cost of the photo mask in moving from a 90 nm to a 65 nm process.

As shown in Tables V and VI below, at the 65nm node, the COO savings are even greater with

the S-FIL/R process, which exhibit a 68% savings for contacts and 61% savings for the Dual Damascene process. This improvement is primarily driven by the material (i.e. template) costs.

Contacts at the 65 nm Node

Parameter	**Photolithography**	**S-FIL/R**
Tool Price ($)	25 M[7]	10 M
Installation Cost ($)[8]	1 M	0.5 M
Mask/Template Price ($)	100,000	27,500
Effective Throughput (WPH)	60	50
Mask/Template Usage	2000 wafers	2000 wafers
COO	**$65.86**	**$20.78**

Dual Damascene Process at the 65 nm Node

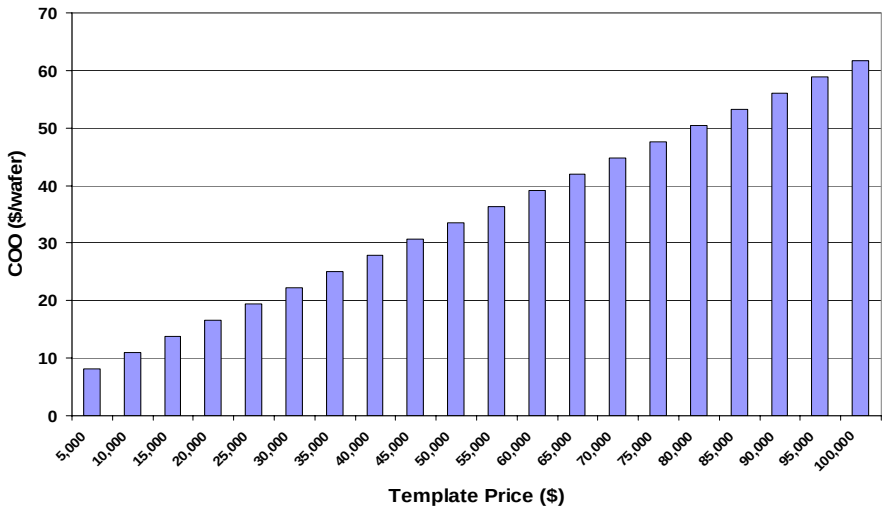
Parameter	**Photolithography**	**S-FIL/R**
Tool Price ($)	25 M[9]	10 M
Installation Cost ($)[10]	1 M	0.5 M
Mask/Template Price ($)	**100,000 (1 for via and 1 for trench)**	**82,500 (2-tier template)**
Effective Throughput (WPH)	60	50
Mask/Template Usage	2000 wafers	2000 wafers
COO	**$131.72**	**$51.81**

Sensitivity Analysis

One primary issue in calculating COO is the assumptions associated with materials costs, throughput, and process life of an emerging technology like imprint lithography. While a strong effort has been made in this paper to accurately represent the COO of S-FIL/R that is consistent with the current state of the technology, it is prudent to investigate the sensitivity of the COO model, with respect to certain key factors including imprint template price, template usage, and tool throughput.

Template Price

A sensitivity analysis varying the template price from $ 5000 to $ 100,000 is conducted for the contacts scenario (i.e. single template scenario).



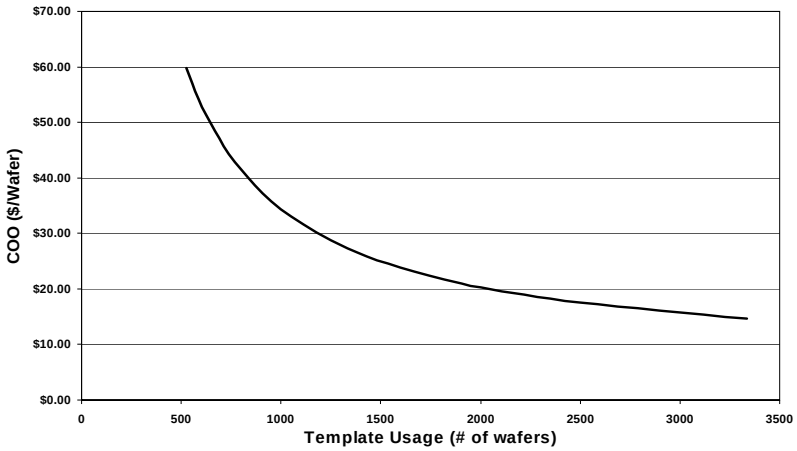
It is clear that the template cost plays a crucial role in the COO of S-FIL/R. However the above

[7] Does not include resist coating/baking/developing equipment
[8] Installation Cost is estimated at 5% of equipment purchase costs. Transportation costs have not been included
[9] Does not include resist coating/baking/developing equipment
[10] Installation Cost is estimated at 5% of equipment purchase costs. Transportation costs have not been included

illustration raises several interesting possibilities. At low template pricing (e.g. assuming minimal inspection), the possibility of using S-FIL/R for generating prototypes of new chip designs for validation as well experimenting with new devices at higher node levels would be immense. Quick turnaround of prototype designs at low cost can considerably shorten time to market for new products. This could result in significant benefits to companies, in terms of competitive advantages not accounted for in the COO calculation.

Template Usage

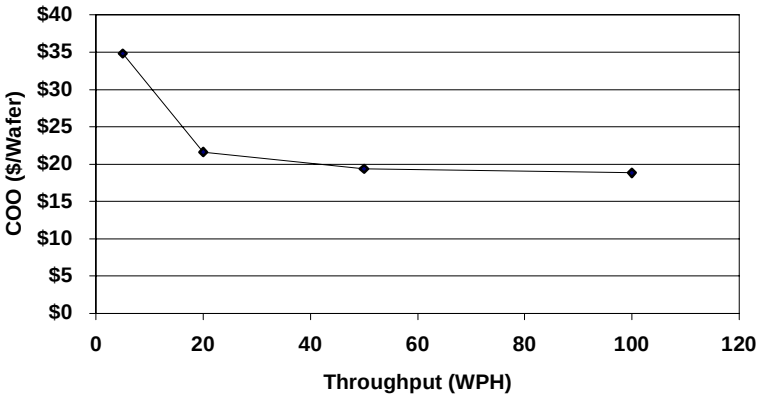
A sensitivity analysis varying the template usage from 500 wafers to 3000 wafers is conducted for the 90 nm contacts scenario (i.e. a single tier template).



Even at low template usage estimates, the COO of imprint technology is very attractive. In recent years, low volume applications such as ASICs have lost ground to more standardized designs such as FPGAs and hybrid ASICs. The primary reason being the high non-recurring engineering costs coupled with the high cost of manufacturing, such as the high cost of masks and photo tools. However, disruptive lithography technologies like S-FIL/R can make such applications attractive once again.

S-FIL/R Tool Throughput

A sensitivity analysis varying the SFIL/R tool throughput from 5 WPH to 100 WPH is conducted for the contacts scenario. As the S-FIL/R tool throughput is varied, the tool price is also adjusted from $ 3M to $ 20 M to reflect the additional cost of satisfying the respective throughput specification.



The COO of S-FIL/R is still very attractive at low throughputs, thus providing a significant advantage for applications such as chip prototyping and R&D, cited above. Also at higher throughputs (>20 WPH) the COO of S-FIL/R is a clear winner. The results in the above table demonstrate that S-FIL/R provides immense value as it evolves from lower

throughput tools to high throughput, production-oriented tools.

Conclusions

The paper demonstrates the clear advantage that S-FIL/R provides in terms of COO over competing photolithography techniques, especially in the sub 90 nm node regime for applications such as contacts and dual damascene processes. Using COO sensitivity analyses around uncertain cost parameters, the authors show that S-FIL/R is an attractive lithography technology for high-resolution applications.

Acknowledgements

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References

[1] "193 nm Immersion Lithography Rated Suitable for Fab Evaluation", Third Immersion Workshop sponsored by International SEMATECH (ISMT), January 27th 2004 (source: http://www.sematech.org/corporate/news/releases/20040127.htm)
[2] Hara, Yoshiko, "Nikon launches EUV lithography development", EE Times, January 14th 2004
[3] Resnick, Doug, Willson, Grant, Sreenivasan, S.V., "Making an Imprint", SPIE OE Magazine, August 2003
[4] Sreenivasan, S. V, et al, "Reverse Tone Bi-Layer Etch in UV Nanoimprint Lithography", Micro Magazine, Jan/Feb 2005.
[5] Semi roadmap adds imprint, maskless lithography, EE Times, December 2003
[6]M. Stewart, et al, "Direct imprinting of dielectric materials for dual damascene processing" SPIE Microlithography Conference, March 2005.
[7] James, Geoffrey, " Navigating 65 nm Design Limits", Electronics Design Chain, Spring 2004

Editor's Note: This paper was based on a poster session first presented at SPIE 2005.

Call for Papers ICICDT

May I please bring to your attention the upcoming 2nd International Conference on Integrated Circuit Design and Technology, ICICDT, Austin, TX, May 9-11, 2005. Please also visit the conference website at http://www.ICICDT.org.

If you should have questions regarding ICICDT 2005 do not hesitate to contact me.

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A WIP-Centered View of the Fab: Part 1: WIP States

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Introduction

A common approach in monitoring fab performance is to take a tool-centered approach. This involves measuring overall equipment effectiveness (OEE) for bottlenecks, recording A20 and A80 and downtime characteristics, and tracking the time that tools spend in particular states (especially the dreaded "standby with WIP waiting" state). The tool centered view is very important in running a fab, because the individual tools are so expensive.

In this article, however, we would like to propose a parallel WIP-centered view of the fab. That is, for an individual lot, we can look at the time that the lot spends in various states (processing, waiting, traveling, etc.), and these will be analogous to tool states. We can also use the WIP state information to calculate a performance measure parallel to OEE, called Overall WIP Effectiveness. We believe that understanding exactly where lots are spending their time is an important step in improving cycle time, and that WIP states and overall WIP effectiveness have the potential to add a great deal to the understanding of the fab.

In Part I (this issue) we will define and discuss standardized WIP states. In a companion article (Part II) we will define the performance measure Overall WIP Effectiveness.

WIP States

As a lot goes through the fab, it spends time in a variety of states. We believe that by measuring this time and grouping it into set categories, fabs can learn a great deal about how lots are spending their time. This, of course, is the first step towards reducing the time spent in less productive categories, and hence improving cycle time. As a first pass, we propose that lot time be broken into the following six WIP states:

- Processing
- In Queue
- On Hold
- Post-Processing (e.g. waiting for unload)
- Traveling
- In Crib (extended hold, or storage near the end of the line)

The difficulty of capturing time in each state will vary from fab to fab. At the most basic level, if Begin Run (start processing a lot on a tool) and Move Out (finished processing, move to next step) transactions are logged, then it is possible to split time into two states: process time and queue time. Generally holds and crib time will be logged independently, making it possible to split hold time and crib time out as well. If End Run is logged separately from Move Out (say by tool automation), then we can split queue time into post-process queue time and regular queue time. Splitting out travel time will also be possible if transfer times are logged in detail.

Two examples of potential WIP state charts are included in the PDF version. One shows the total cycle time for each lot in days, broken into the six states described above. The other displays the WIP states as a percentage of total time for each lot. To request a copy of the PDF version, and/or to switch to the PDF version for future issues, email your request to Jennifer.Robinson@fabtime.com.

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Extensions to the Basic WIP States

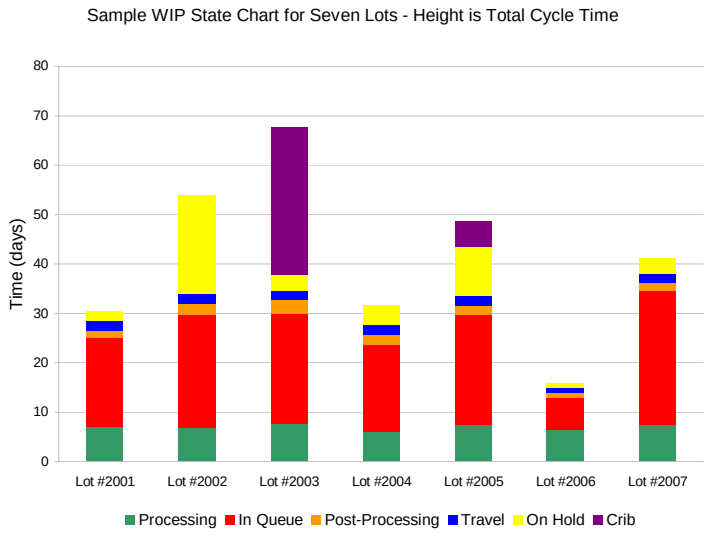
Much of the benefit in having a set of common WIP states lies in having there be a few, readily-defined states. This is true of the SEMI E10 tool states, of which there are six primary states. However, we do have to decide how to handle several other special cases.

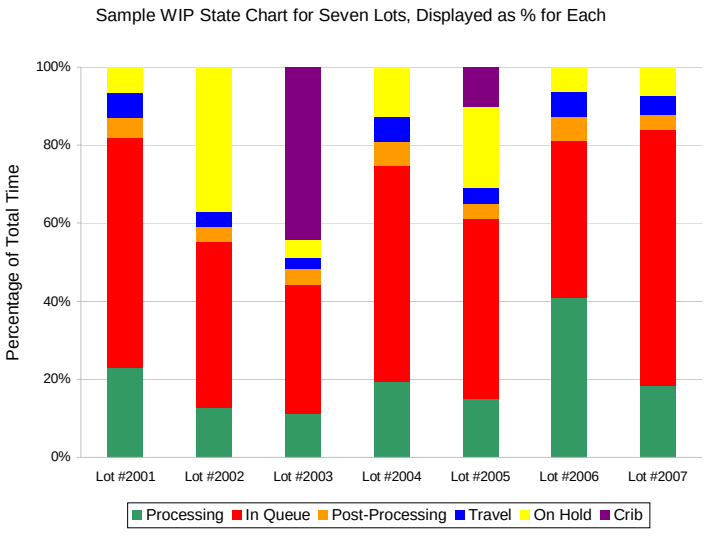
Rework: We would, naturally, like to minimize the time that lots spend being reworked. Therefore, it may be necessary to break up the process time above into processing - regular and processing - rework. Further, we need to account for rework parents and children in some way. The simplest thing is probably to only measure the states for the parent (primary lot), but to count the time spent waiting for the rework child as processing - rework (since part of the lot is processing, but at a rework operation).

Speed Losses: It's fairly easy to measure actual process time for a lot at an operation, provided Begin Run and end run transactions are both recorded. (If End Run is not logged separately from Move Out, then Begin Run to Move Out provides an estimate of process time). However, this alone will not tell us anything about how that actual process time compares to the planned process time for the operation. This could be handled by adding a third processing category, called processing - speed loss. This would require the creation of a virtual transaction to mark the end of the planned process time. The time between that time and the actual End Run time would be recorded as processing - speed loss. However, we believe that capturing this is not as important as capturing the basic states, as defined in the previous section.

Load Time / Unload Time: Load/unload time can be separated out from process time. However, since it is generally required in order to complete an operation, we recommend breaking it out from process time only if a particular load time reduction project is underway (and even then only for key tools).

Setup Time: When viewing tool states, setup/qualification time is generally treated as part of scheduled downtime. Setup is time that the tool is unavailable, but it is "planned" in the sense that the tool dispatching policy drives how much setup time is required. Qualification time at the end of maintenance events is similarly planned. In the case of WIP states, setup time should probably just be treated as part of queue time (since the tool is unavailable for the lot during the setup, and the setup time is not inherently part of the lot's process time).





Further Extensions to WIP States - Breaking Down Time in Queue

To even better understand where lots are spending time, and why, we might break the time in queue down into several smaller buckets:

In Queue - Waiting for Other Lots to Finish (another lot is being processed on the tool, and/or the lot is not at the front of the queue)
In Queue - Waiting for Operator (the lot is at the front of the queue, and the tool is available, but no operator is available)
In Queue - Waiting for Scheduled Down (the lot is at the front of the queue, but the tool is down for maintenance)
In Queue - Waiting for Unscheduled Down (the lot is at the front of the queue, but the tool is in an unscheduled downtime).

Note that we only count time as waiting for operator or downtime when the lot is at the front of the queue. This is because if the lot is further back in the queue, it wouldn't be processed next, even if the tool were available. This is queue time waiting for other lots to finish. This type of queue time is generally driven by equipment utilization (the busier the tool, the more likely that other lots will be ahead of this lot in the queue).

These additional sub-states could provide useful additional information about why lots spend time in queue. However, they are more difficult to measure, because they require knowing which lot is at the front of the queue at all times, even when the tool is not available. Because multiple tools may be qualified to run a particular lot, this can get tricky. Therefore, as above, we recommend starting with the basis states outlined previously, and only breaking up the queue time into sub-states for key tools, or where automated tracking systems make this data to capture.

Conclusions

In the classic tool-centered view of the fab, tool performance is measured using tool state charts (often following the E10 standard for definition of the tool states). This approach is very helpful in providing direction for equipment improvement programs. What we have done in this article is propose a similar set of states that apply to the time that each lot spends in the fab. That is, we will break up a lot's history, and measure how much time it spends in several basic states such as queue, process, post-process, hold, transport, and crib. Having ready access to this information can help fabs to identify opportunities for improvement. Having a graphical representation of the WIP state data will in turn help to track and visualize the improvements. The natural extension to this, development of an overall WIP effectiveness metric, will be discussed in the next issue.

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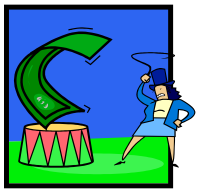

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Wright Williams & Kelly Names Selastar Sales Agent

Adds Japan to its Global Expansion of Sales and Service

December 15, 2004 (Pleasanton, CA) –Wright Williams & Kelly, Inc. (WWK), a cost & productivity management software and consulting services company, announced today the naming of Selastar Corporation as its sales agent covering Japan. This appointment represents the continuation of WWK's strategic vision to provide increased sales and service support in close proximity to all of its customers, world-wide.

"Selastar Corporation was selected to support our established and growing installed base in Japan based on their many years of successfully meeting the needs of their clients," states David W. Jimenez, WWK's President. "They combine a comprehensive understanding of the region's high-tech climate with an extensive background in software sales and support. We look forward to working with them to support our existing installed base and expanding the application of our software products and services."

"We are pleased to begin representing WWK and its product line. Their products and services fit nicely with our offerings in other software and hardware areas," says Archie Ishikawa, President of Selastar Corporation. "We see a large demand for software tools and consulting services designed to help optimize manufacturing costs and productivity. WWK will help keep our clients at the forefront of cost competitive operations."

Selastar Corporation is a privately held company specializing in serving the Japanese semiconductor, LCD and other microelectronics-related markets. The company's product line includes software tools, instrumentation and components which are technologically innovative and capable of significantly enhancing the level of productivity in factory operations. The company's seasoned management team, consisting of staff who were formerly with TEL and Innotech, maintains a wide range of customer contacts and brings years of experience in distribution of such products in Japan.

WWK Signs IP Acquisition Agreement for Ultra-Fast, Resource Driven Simulation Technology

February 22, 2005 (Pleasanton, CA) –Wright Williams & Kelly, Inc. (WWK), a cost & productivity management software and consulting services company, announced today it has reached an agreement with Dr. Lee Schruben of the University of California, Berkeley for the acquisition of intellectual property (IP) involving ultra-fast, resource driven (RD) manufacturing simulation. This technique has been proven to be up to 70x faster than Job Driven (JD) simulation approaches.

Wright Williams & Kelly, Inc. has a long history of providing fast simulators to industrial clients. WWK's Factory Explorer® is based on the same "event-graph" technique employed by Dr. Schruben but was designed to provide the additional details required in job driven simulation. Even so, Factory Explorer® has been benchmarked with industry standard data sets to be more than ten times faster than other job driven simulators. Additionally, simulation speeds in excess of 3.5 million lot moves/minute are achieved with modest laptop computers (1.8 GHz, 256Mb DRAM) running standard Windows operating systems.

"We are very pleased to reach this agreement with Dr. Schruben," states David Jimenez, President of WWK. "The ability to further reduce execution times on complex manufacturing simulations is vital to our client base. With competing products, you are forced to choose between the multiple runs needed to map out a response surface and the fact that the answer may be too late to drive critical business decisions. With the addition of Dr. Schruben's IP to our product portfolio, we believe that our clients will no longer need to make that trade-off."

WWK further indicated it is looking to partner with potential end users of this technology to ensure that the resulting commercialization meets industry needs. Potential further enhancements include the ability to import data from other simulation platforms to provide easy access to the new RD simulator.

"I expect that the speed advantages from using event relationship graphs to create fab and tool simulations will have a major impact on the industrial use of simulation"

Dr. Lee Schruben is Chairman of the Department of Industrial Engineering and Operations Research and a Chancellor's Professor at the University of California, Berkeley. Prior to joining the faculty at Berkeley, he was on the Operations Research and Industrial Engineering faculty at Cornell where he held the A. Schultz Professorship in Engineering. He received his PhD from Yale and is a Fellow of the Institute for Management Science and Operations Research. Professor Schruben's research interests are in simulation modeling and analysis methodologies with a broad range of applications including biopharmaceutical production and supply chains, semiconductor manufacturing and equipment modeling, entertainment and banking, food services, and golf course design and operation. The Semiconductor Research Corporation, National Science Foundation, the Navy and Air Force, Intel, ATT, General Electric, Bethlehem Steel, Digital Equipment, Battelle, Kodak and the National Research Council have been sponsors of his research.

Call for Papers: MASM 2005

We would like to cordially invite you to submit a paper to the International Conference on Modeling and Analysis of Semiconductor Manufacturing (MASM 2005), to be held in Singapore on 6/7 October 2005 at the Suntec International Convention & Exhibition Centre.

Full Paper Submission Due Date: 15 May 2005

Notification of Acceptance: 1 July 2005

Camera-Ready Due Date: 15 August 2005

MASM 2005 will be a forum for the exchange of ideas and best practices between researchers and practitioners from around the world involved in modeling and analysis. While we seek to know what's going on within the semiconductor industry, neither presenters nor attendees need to be in the semiconductor industry to participate. Any methodologies, research, and/or applications from other industries, as well, that might also be utilized for the semiconductor industry, will be considered relevant for this conference.

The conference includes tutorials, tea breaks, lunches and related software demonstrations. An international panel supervises each track. A broad range of papers is sought, including theoretical developments, applied research and case studies. Interested individuals within academia, government agencies, equipment suppliers, manufacturers, students, contractors, and other interested parties are encouraged to participate.

The conference will be built around the following five tracks:
1. Equipment Productivity
2. Operational Modeling and Simulation
3. Statistical Methods
4. Supply Chain Management
5. Enabling Computing Techniques

Track Information:
http://www.simtech.a-star.edu.sg/masm2005/ti.htm

Conference Committee:
http://www.simtech.a-star.edu.sg/masm2005/committee.htm

Paper Submission and Review Schedule:
http://www.simtech.a-star.edu.sg/masm2005/cfp.htm

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Peter Lendermann (MASM 2005 General Chair)
John Fowler (MASM 2005 Programme Chair)

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