Information Exchange For Your Application & Use of Cost Modeling

APPLIED Co$t MODELING

Join WWK at SEMICON West in Celebrating Our 15th Anniversary

Volume 12. Issue 3

Inside

Spring 2006

ISSN 1094-9739

Cost of Ownership Impacts on LPCVD Nitride Deposition

Summary of Detailed Results

David W. Jimenez
Wright Williams & Kelly, Inc.

Background

For more than 20 years the semiconductor industry has sought a solution to the acute problems that accompany the use of quartz and silicon carbide (SiC) in furnace processes. These processes, including high temperature anneal, diffusion and deposition processing, make up to 30 percent of the major process steps in wafer manufacturing.

While recent improvements in furnace cleaning have helped to remediate particle defects induced by quartz or SiC consumables, engineers still have not achieved the overall reduction of defect rates required for state-of-the-art manufacturing environments. Moreover, the cleaning process is costly; capital, chemicals and the necessary environmental safeguards drive up the cost of ownership (COO).

Additionally, integrated circuit (IC) manufacturers must cope with trace metal contamination, “slip” due to differences in the Coefficient of Thermal Expansion (CTE) between wafer support consumables and the wafer, and consumables’ structural stability in the high-temperature processes.

[Continued on Page 3]

Editorial Board

Publisher

Published quarterly by:

Wright Williams & Kelly, Inc.
6200 Stoneridge Mall Road
3rd Floor
Pleasanton, CA 94588

Phone 925-399-6246
Fax 925-396-6174
E-mail support@wwk.com

Available at:
http://www.wwk.com
Select "Newsletter"

Calendar of Events

June 2006

14-16 **FPD Taiwan**
Taipei, Taiwan

July 2006

11-13 **SEMICON West (WWK booth #2716)**
Moscone Hall South, San Francisco, CA
PLEASE NOTE NEW BOOTH NUMBER

13 **Understanding & Using Cost of Ownership**
Marriott Hotel, San Francisco, CA

August 2006

10-12 **Emerging Information Technology Conference**
Univ. of Texas, Richardson, TX

September 2006

11-13 **SEMICON Taiwan**
Taipei, Taiwan

October 2006

9-11 **ISMI Symposium on Manufacturing Effectiveness**
Austin, TX

10-11 **Industry Strategy and Technology Forum**
Yokohama, Japan

November 2006

5-8 **International Trade Partners**
Kohala Coast, Hawaii

December 2006

3-6 **Winter Simulation Conference**
Monterey Conference Center
Monterey, CA

Now, given the demanding characteristics of advanced IC device processing as the industry continues to both shrink device architectures and move to 300-mm wafers, the need for a solution to these problems grows even greater.

To address these problems, Integrated Materials recently introduced its patented SiFusion™ technology that allows for the manufacture of pure poly silicon furnaceware. SiFusion is the first proven application of poly silicon furnaceware as an alternative to current quartz and SiC consumables. The suite of SiFusion products includes furnace boats, liners, injectors and pedestals. These products are designed for furnaces from the major capital equipment suppliers, Tokyo Electron, Hitachi-Kokusai, ASM, Aviza and others.

With the introduction of SiFusion as a viable alternative to traditional consumables, there is an opportunity to examine the COO for all three furnace consumable materials. Thus, Integrated Materials retained a COO modeling expert, Wright Williams & Kelly, Inc. (WWK), to examine pure poly silicon furnaceware compared to quartz and SiC in both 200-mm and the 300-mm environments.

Cost of Ownership Overview and Methodology

WWK created an extensive matrix to examine materials combinations for both 200-mm and 300-mm low pressure chemical vapor deposition (LPCVD) nitride applications. The materials examined were quartz, SiC, and pure poly silicon (SiFusion). These materials were examined for both boat and liner applications as well as external and in situ clean (300-mm). The fundamental parameters for the vertical furnace remained constant regardless of materials used but were updated for differences in wafer size.

The objective of this project was to estimate the operational cost differences resulting from these material combinations.

For the following analyses, WWK utilized TWO COOL®, the semiconductor industry's COO and overall equipment efficiency (OEE) standard. TWO COOL is the only software to comply with Semiconductor Equipment and Materials International (SEMI) Standards E10, E35, and E79.

200-mm COO Cost Drivers

Examination of the detailed TWO COOL COO models for each material combination highlights the main cost driver differences. In the case of quartz boats and liners, the main cost drivers, aside from the equipment factors that are the same for all analyses, are the increased frequency of cleaning and the resultant decreases in equipment utilization and high cleaning costs, and the short useful life. Some of these higher costs are offset by the relatively low price for these parts.

SiC components provided an interesting analysis in that the combination of an SiC boat and a quartz liner had a lower COO than the SiC/SiC combination, which had the highest cost of all the materials examined. This is based on the fact that SiC boats require the same amount of cleaning compared to quartz, cost significantly more to purchase, but last significantly longer. SiC liners also have to be cleaned at the same frequency as quartz. The significantly higher purchase price for SiC is mitigated somewhat by their long potential life. However, the high cleaning frequencies place these high-price materials at risk of breakage on a regular basis.

ISSN 1094-9739

SiFusion boats and liners provided the lowest COO by a substantial margin. This was achieved through the total elimination of routine cleanings for both components. This increased the Production Utilization Capability by 9 percent and reduced lifetime costs by almost $900k. The higher purchase price of the SiFusion material is more than offset by its long life and drastically reduced risk of breakage.

Based on these results, it is estimated that the payback period for the SiFusion boat is nine weeks ([$18,500 - $2,500]/[[$2.65 - $2.19] x 3,984 wafers out per week]) compared to quartz/quartz and shorter compared to SiC/quartz. Further, the SiFusion liner has a payback period compared to quartz of 70 weeks.

300-mm COO Cost Drivers

Examination of the detailed TWO COOL COO models for each material combination highlights the main cost driver differences. In the case of quartz boats and liners, the main cost drivers are the frequency of cleaning and the resultant decreases in equipment utilization and high cleaning costs, and short useful life. Some of these higher costs are offset by the relatively low price for these parts. The use of in situ cleaning provided no advantage due to the high cost of cleaning materials. The potential advantages for in situ cleaning are only seen when the cleaning frequency is well below 10 µm. This was true for all the cases examined in this report.

SiC components provided the three highest COO results. The combination of an SiC boat and a quartz liner had a lower COO than the SiC/SiC combination and in situ cleaning, again, increased costs. This is based on the fact that SiC liners have to be cleaned the same as quartz but have a significantly higher purchase price. The purchase price for SiC is mitigated by their long potential life. However, the high cleaning frequencies place these high-price materials at risk of breakage on a regular basis.

SiFusion boats and liners provided the lowest COO by a substantial margin. This was achieved through the total elimination of cleanings for both components. This increased the Production Utilization Capability by over 7 percent and reduced lifetime costs by almost $2 million compared to SiC/SiC. The higher purchase price of the SiFusion material is more than offset by its long life and drastically reduced risk of breakage. Based on these results, it is estimated that the payback period for the SiFusion boat is 40 weeks ([$48,000 - $5,000]/[[$3.58 - $3.30] x 3,871 wafers out per week]) compared to quartz/quartz and shorter compared to SiC/quartz. Further, the SiFusion liner has a payback period compared to quartz of 33 weeks.

Conclusions

Integrated Materials proposes these advantages for IC manufacturers when using SiFusion-produced pure poly silicon furnaceware, as compared to quartz or SiC consumables:

1. No other material used in semiconductor processes can compare to the purity of Integrated Materials' poly silicon fixtures. Integrated Materials components are clean to <1.0 E10 / cm^2 for all trace metals.

2. In LPCVD processes, the close match of CTE between Integrated Materials' component and the LPCVD film and Integrated Materials' patented surface preparation result in the elimination of fixture-generated particles.

Long-term production use of Integrated Materials' pure poly silicon boats in LPCVD nitride confirms that no scheduled cleaning is needed. Benefits from the elimination of cleaning include:

1. Significant cost savings by the elimination of HF and other chemicals used for cleaning.

2. Environmental benefits from the elimination of toxic chemical disposal.

3. Fewer process interventions resulting in more stable furnace operation.

At temperatures to 1375°C, Integrated Materials' pure poly silicon boats do not deform. Integrated Materials' poly silicon products are thermal shock resistant: they maintain their mechanical tolerances at temperatures far above those experienced by IC wafers. SiFusion fixtures exposed to 1350°C in excess of 12 months have maintained tolerances and exhibited no structural degeneration from their original form.

The CTE for the wafer and Integrated Materials' poly silicon boat match, allowing for increased thermal ramp rates and reduced thermal stabilization times while eliminating damage to the wafer and eliminating boat-inducted slip. Integrated Materials' poly silicon boats are transparent to infrared (IR) which reduces thermal "shadowing" and causes more uniform heating within the hot-zone.

Integrated Materials' precision manufacturing tolerances provide for a more efficient robotic interface that speeds up wafer load/unload time. Integrated Materials' precision standards provide for true "plug-and-play" use.

Integrated Materials' pure poly silicon components deliver equal or longer useful life than those made from SiC.

To download a full copy of this extensive twenty-two page research report, please visit the SiFusion web site at:

http://www.sifusion.com/nitride/

COO Projects for SEMICON West

If you would like to take advantage of WWK's expert cost of ownership (COO) modeling services in time for SEMICON West, there is still time to generate the data you need to support your product positioning.

For COO and overall equipment efficiency (OEE) applications, WWK offers consulting services including data collection, application development, and results analysis and recommendation. To assist in results distribution, all analyses utilize the world's most accepted COO and OEE software, TWO COOL®. These same services are also offered for cost, risk, and return on investment (ROI) analyses.

Factory level modeling requires a broader base of resources to address data collection and entry, model verification and validation, and results analysis and recommendation. Factory modeling includes both static (Factory Commander®) and dynamic (Factory Explorer®) approaches to capacity, resources, costs, and revenues. WWK has proven expertise in the areas of factory cycle time reduction, constraints management, and build-to-stock/build-to-order/assemble-to-order production systems.

ISSN 1094-9739

Strategic Marketing Associates & Wright Williams & Kelly, Inc.
Semiconductor Equipment Forecast Shows Softening Litho Market in 2008

EquipmentFutures™ Quarterly Subscription Provides Unit and Revenue Forecasts by Equipment Type

May 25, 2006 (Pleasanton, CA) – Strategic Marketing Associates (SMA) and Wright Williams & Kelly, Inc. (WWK) announced today the availability of EquipmentFutures™, a quarterly forecast of equipment sales in units and dollars for six major equipment types. EquipmentFutures™ incorporates information from short-term semiconductor activity forecasts from more than 200 fabs, long-term industry forecasts, consumer electronics demand, and industry roadmaps and integrates that data with best-in-class wafer fab simulation to provide highly accurate equipment forecasts. EquipmentFutures™ reflects both productivity changes and semiconductor processing trends as the industry faces the continuing challenges of Moore's Law. EquipmentFutures™ can be purchased on the SMA web site at www.scfab.com.

"EquipmentFutures™ allows us to leverage our multi-year relationship with SMA by combining their worldwide fab data with the modeling capabilities of WWK," stated Daren Dance, WWK's Vice President of Technology. "EquipmentFutures™ is unique in that it incorporates both top-down and bottoms-up forecasts to uncover any discontinuities and allows consideration of equipment specific trends. We are also leveraging our relationships with Wall Street custom research houses to incorporate forecasts of end market demand that are currently only available to large mutual and hedge funds."

"For example, our analysis suggests that the lithography equipment market will soften in 2008. A likely scenario will have leading edge manufacturers placing initial orders for next generation lithography (NGL) equipment, but then we expect a pause in purchasing to allow evaluation of results. After the pause, chip companies will commit to production purchases."

"We are excited to add this unique forecast to our offerings," said George Burns, President of SMA. "When the end user combines the data from EquipmentFutures™ with FabFutures™ they will not only be able to know what fabs will be built and when, but they will also be able to generate equipment lists in each fab. This is a must have for every equipment company regardless of size."

EquipmentFutures™ covers six individual equipment groupings: lithography, chemical-mechanical polishing (CMP), etch & clean, implant & thermal processing, metal deposition, and non-metal deposition. Each module contains information on revenues and unit volumes (conservative, median, and optimistic) as well as projected average selling price (ASP) on a quarterly basis for five years. Information on the impact of the International Technology Roadmap for Semiconductors (ITRS) and other market considerations are included as background to the forecast. The lithography report is available immediately and the other reports will be released over the next two weeks.

EquipmentFutures™ is unique compared to other forecasting services in that it not only takes into consideration market research on semiconductor and equipment sales but also end market demand. This data is then analyzed using WWK's sophisticated factory planning software and proprietary process flow data sets. The result is a convergence of top-down forecasts and bottoms-up economic modeling.

SMA provides the industry with comprehensive and accurate data about wafer fabs and summary information about key industry trends. SMA has developed a suite of fab information products including 'The Quarterly Spot Report' on Semiconductor Fab Products, 'International Wafer Fab News', 'Fab Expenditures: The Next 18 Months', 'The Fab Construction Monitor: The Next 18 Months', 'The 300-mm Fab Report' and the newly introduced 'FabFutures' and 'Fab TimeLine'.

Advantages of a Factory/Global Perspective in Test Floor Optimization

David W. Jimenez, Wright Williams & Kelly, Inc

Overview

This paper looks at the progression of cost and capacity modeling from the step or component level to full factory discrete-event simulation. The latter is used to examine the potential benefits of a flexible test architecture like the one described by the Global OPENSTAR™[1] specification.

Step/Component Level Cost of Ownership (COO)

Semiconductor Equipment and Materials International (SEMI) E35 defines COO as the full cost of embedding, operating, and decommissioning, in a factory environment, a system needed to accommodate a required volume. The significant COO inputs for test include:

- Equipment cost
- Operating cost
- Yield
- Down time
- Throughput rate
- Value of completed unit
- Cost of discarding a good unit
- Cost of shipping a bad unit

These factors are combined in the COO equation:

$$COO = \frac{CF + CV + CY}{TPT * L * Y * U}$$

Where:

COO = Cost of Ownership for Test
CF = Fixed Cost
CV = Variable Cost
CY = Cost of Yield Loss
TPT = Throughput Rate
L = Lifetime of test system
Y = Yield
U = Utilization

Fixed costs are incurred once during the life of the system and are associated with the acquisition and installation of equipment. Fixed costs include costs such as equipment purchase, installation and setup, facility modifications, initial training, and initial calibration costs. Variable costs are

[1] The Semiconductor Test Consortium is a not-for-profit industry group formed to develop a new Open Semiconductor Test Platform. Its main objective is the development and implementation of the Open Semiconductor Test Architecture (OPENSTAR™). More information is available at www.semitest.org.

ISSN 1094-9739

incurred on an accrued basis. Variable costs such as material, labor, repair, standards, recalibration, utility, and overhead expenses are costs that are incurred during equipment operation. Cost of yield loss is the value of scrap caused by the test step. Scrap identified at test but caused by prior processing is part of the prior process tool COO. Thus, yield losses caused by the test tool must be clearly separated from prior losses. Yield losses caused by the test equipment are assumed to be zero as shown by the values in Figure 2 where the with and without scrap values are the same. The sum of costs form the numerator of the COO equation.

The denominator of the COO equation is an estimate of the number of good units produced during the life of the system. Throughput rate is based on measurement and handling times such as sample preparation, loading and unloading, reporting, and other overhead operation. It excludes training, repair, and calibration times since these are included in utilization. Yield may be defined as the ratio of good units compared to the total number of units produced, including rework. Utilization is the ratio of actual usage compared to total available time. Utilization includes repair and maintenance time, both scheduled and unscheduled; setup and calibration time; and standby time. It shows the impact of non-productive time on cost and normalizes ideal throughput to a realistic estimate. Utilization should be estimated using SEMI E10 definitions for availability, reliability and maintainability.

The application of cost of ownership to test floor operations requires detailed data on equipment and test requirements. The focus is on activities that drive costs at the step level. COO is most effective for local optimization where management responsibilities are also local. The COO model is typically either of a component (tester, handler, or prober) or an aggregate test cell. The advantage of this approach is that the data is usually under the control of a single engineer and easy to obtain. The disadvantage is that the model ignores the interactions of components or other steps on the test floor.

Figure 1 shows a common TWO COOL® COO sensitivity analysis to measure the impact of useful system life on costs.

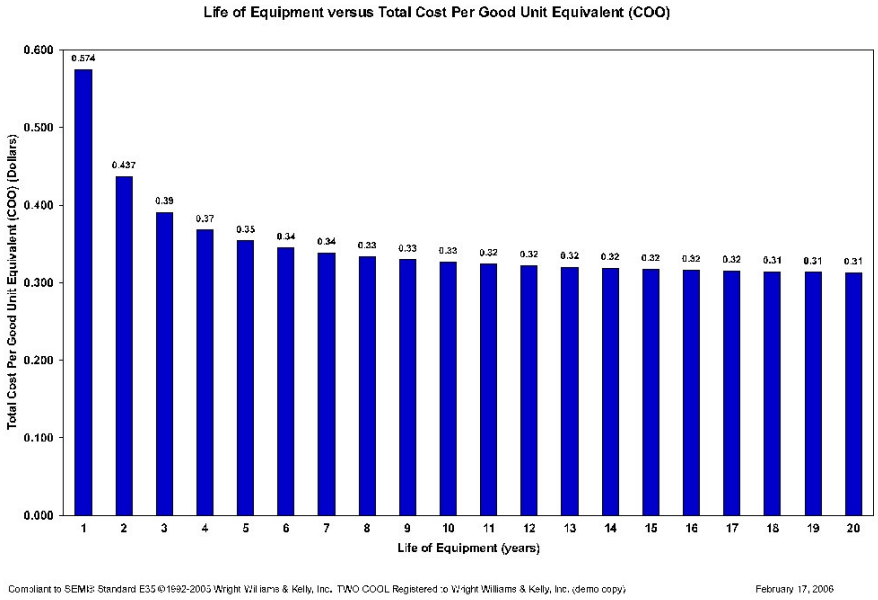


Figure 1: Life extendibility impacts on COO

Test Cell Level Cost of Ownership

The next step in the evolution of cost modeling for test floor operations provides an integrated approach that maintains the details of component level analysis but adds the ability to look at the test system on a holistic basis.

This approach leverages details on equipment and test requirements while focusing is on activities that drive costs and capacity at the cell level. This approach is effective for local optimization where responsibilities are also local. The model is an aggregate test cell based on component details. The advantage is that components can be changed out rapidly to find the optimal test cell. The disadvantage is that the model ignores the interactions of other steps on the test floor.

Figure 2 is a summary report based on the aggregate costs of fifteen test cells needed to meet the test floor capacity demands.

Management Summary Report

Originator:	WWK	Company:	WWK
Test Cell:	Example 2	Log Point:	
Description:	Parallel Probers with Offline Inker		
Comments:			

		Cost per Device	
Test Cell Name : Example 2			
Cost of Systems	23,250,000.00		Dollars
Test Cells Required:	15.00		
Average Utilization	47.10		%
Type I (Alpha) Error	0.00		%
Type II (Beta) Error	0.00		%
Cost of Beta Error	0.0000		%
Good Wafer Equivalents Out Per Week	1,000.00		Wafers
Good Wafer Equivalent Cost			
With Scrap	387.4048	1.3689	Dollars
Without Scrap	387.4048	1.3689	Dollars
Initial Product Cost	1,000.0000	3.5336	Dollars
Product Cost at End of Flow	1,387.4048	4.9025	Dollars
Cost Per Productive Minute	38.4330		Dollars
Average Monthly Cost			
With Scrap	1,678,754.07		Dollars
Without Scrap	1,678,754.07		Dollars
Life of Process	7		Years
Fixed Costs	23,676,507.90		Dollars
Fixed Cost Per G.W.E.	64.8671	0.2292	Dollars
Time Based Recurring Costs	117,307,798.64		Dollars
Time Based Recurring Cost Per G.W.E.	321.3912	1.1357	Dollars
Wafer Based Recurring Costs	418,440.00		Dollars
Wafer Based Recurring Cost Per G.W.E.	1.1464	0.0041	Dollars
Total Costs	141,402,746.54		Dollars
Total Cost Per G.W.E. (Cost of Ownership)	387.4048	1.3689	Dollars

Figure 2: Example output from an integrated test cell COO model (PRO COOL®)

Long–Term Factory View

Once the questions being asked exceed the component on isolated test cell environment, the user must broaden their examination to include the influences of all the systems on the test floor. The first step in this approach is to look at impacts from a long-term (i.e., average, non-random) view. This technique allows for the inclusion of multiple products with multiple test flows and times as well as shared resources (equipment and human) across products and flows. The focus is on

activities that drive costs and capacity at the factory and/or test floor level. This is effective for long-term, global optimization where responsibilities are distributed. Typically, the model is high level with aggregated data (availability vs. MTBF). The advantage is that tool groups, process flows, and demand schedules can be changed rapidly to find the optimal test floor operation. The disadvantage is that the model ignores the random nature of failures and product arrivals which can be the most problematic for test floor managers.

Figure 3 highlights the relationships that a factory-level modeling approach can entertain. This layout is representative of a modeling tool such as Factory Commander®.

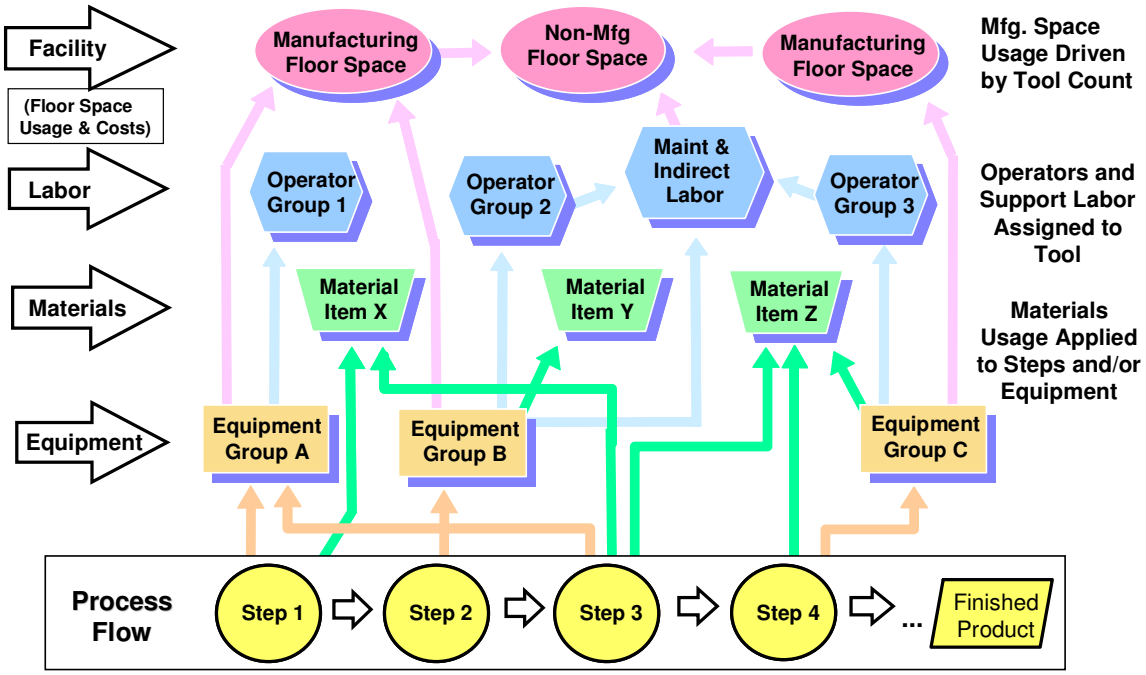
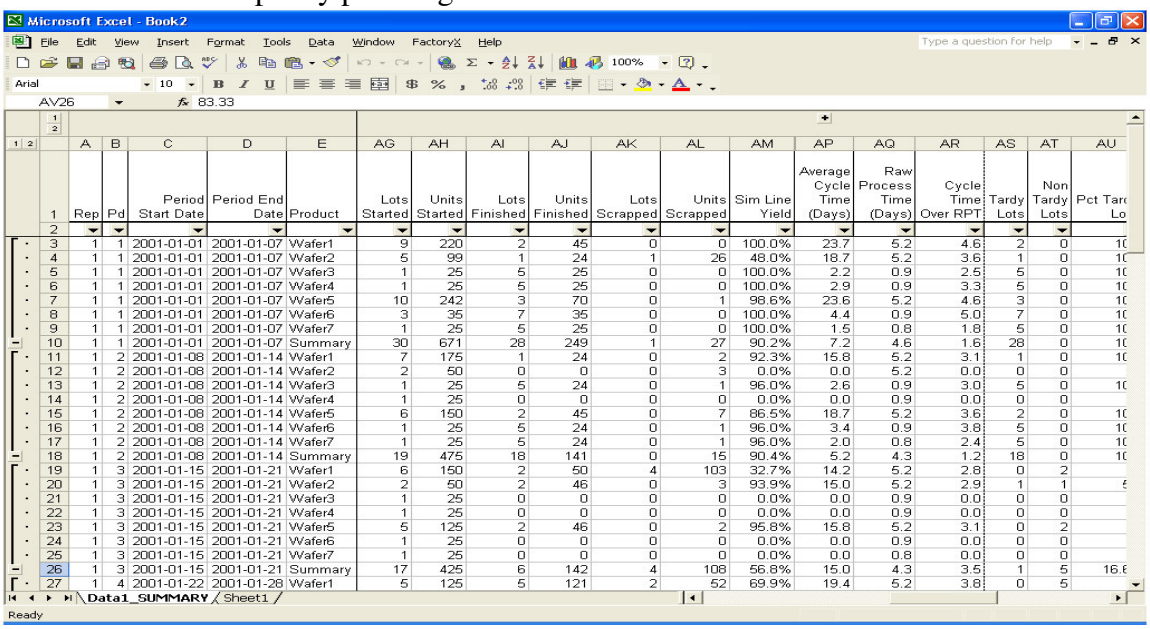


Figure 3: Relationships in a factory level model

Dynamic Factory View

The previous discussion regarding factory-level modeling is sometimes described as best applied to strategic questions, while discrete-event simulation is best applied to the tactical, day-to-day issues that face the test floor manager. This approach simulates the movement of each lot through the factory and/or test floor. It can use random-number generation and data distributions to determine the random nature of resource availability, process/test times, and product arrival rates. With this technique the focus is on activities that drive costs, capacity, work in process (WIP), and cycle time at the test floor level. It is effective for both long-term and short-term, global optimization where responsibilities are distributed. The model can use details or aggregated data and probability (e.g., constants, means, distributions, random-number generation) factors to obtain results that mimic the actual test floor environment. The advantage is the test floor can be linked to the wafer fab to predict the random arrival of product for demand schedules on the test cells. The disadvantage is that the model requires more sophisticated data.

Figure 4 shows results from a simulation demonstrating the random nature of products leaving the wafer fab (weekly units finished by product). This random arrival rate at the test floor creates difficulties in capacity planning for dedicated test architectures.



	A	B	C	D	E	AG	AH	AI	AJ	AK	AL	AM	AP	AQ	AR	AS	AT	AU
1	Rep	Pd	Period Start Date	Period End Date	Product	Lots Started	Units Started	Lots Finished	Units Finished	Lots Scrapped	Units Scrapped	Sim Line Yield	Average Cycle Time (Days)	Raw Process Time (Days)	Cycle Time Over RPT	Tardy Lots	Non Tardy Lots	Pct Tar Lo
2																		
3	1	1	2001-01-01	2001-01-07	Wafer1	9	220	2	45	0	0	100.0%	23.7	5.2	4.6	2	0	1
4	1	1	2001-01-01	2001-01-07	Wafer2	5	99	1	24	1	26	48.0%	18.7	5.2	3.6	1	0	1
5	1	1	2001-01-01	2001-01-07	Wafer3	1	25	5	25	0	0	100.0%	2.2	0.9	2.5	5	0	1
6	1	1	2001-01-01	2001-01-07	Wafer4	1	25	5	25	0	0	100.0%	2.9	0.9	3.3	5	0	1
7	1	1	2001-01-01	2001-01-07	Wafer5	10	242	3	70	0	1	98.6%	23.6	5.2	4.6	3	0	1
8	1	1	2001-01-01	2001-01-07	Wafer6	3	35	7	35	0	0	100.0%	4.4	0.9	5.0	7	0	1
9	1	1	2001-01-01	2001-01-07	Wafer7	1	25	5	25	0	0	100.0%	1.5	0.8	1.8	5	0	1
10	1	1	2001-01-01	2001-01-07	Summary	30	671	28	249	1	27	90.2%	7.2	4.6	1.6	28	0	1
11	1	2	2001-01-08	2001-01-14	Wafer1	7	175	1	24	0	2	92.3%	15.8	5.2	3.1	1	0	1
12	1	2	2001-01-08	2001-01-14	Wafer2	2	50	0	0	0	3	0.0%	0.0	5.2	0.0	0	0	
13	1	2	2001-01-08	2001-01-14	Wafer3	1	25	5	24	0	1	96.0%	2.6	0.9	3.0	5	0	1
14	1	2	2001-01-08	2001-01-14	Wafer4	1	25	0	0	0	0	0.0%	0.0	0.9	0.0	0	0	
15	1	2	2001-01-08	2001-01-14	Wafer5	6	150	2	45	0	7	86.5%	18.7	5.2	3.6	2	0	1
16	1	2	2001-01-08	2001-01-14	Wafer6	1	25	5	24	0	1	96.0%	3.4	0.9	3.8	5	0	1
17	1	2	2001-01-08	2001-01-14	Wafer7	1	25	5	24	0	1	96.0%	2.0	0.8	2.4	5	0	1
18	1	2	2001-01-08	2001-01-14	Summary	19	475	18	141	0	15	90.4%	5.2	4.3	1.2	18	0	1
19	1	3	2001-01-15	2001-01-21	Wafer1	6	150	2	50	4	103	32.7%	14.2	5.2	2.8	0	2	
20	1	3	2001-01-15	2001-01-21	Wafer2	2	50	2	46	0	3	93.9%	15.0	5.2	2.9	1	1	5
21	1	3	2001-01-15	2001-01-21	Wafer3	1	25	0	0	0	0	0.0%	0.0	0.9	0.0	0	0	
22	1	3	2001-01-15	2001-01-21	Wafer4	1	25	0	0	0	0	0.0%	0.0	0.9	0.0	0	0	
23	1	3	2001-01-15	2001-01-21	Wafer5	5	125	2	46	0	2	95.8%	15.8	5.2	3.1	0	2	
24	1	3	2001-01-15	2001-01-21	Wafer6	1	25	0	0	0	0	0.0%	0.0	0.9	0.0	0	0	
25	1	3	2001-01-15	2001-01-21	Wafer7	1	25	0	0	0	0	0.0%	0.0	0.8	0.0	0	0	
26	1	3	2001-01-15	2001-01-21	Summary	17	425	6	142	4	108	56.8%	15.0	4.3	3.5	1	5	16.6
27	1	4	2001-01-22	2001-01-28	Wafer1	5	125	5	121	2	52	69.9%	19.4	5.2	3.8	0	5	

Figure 4: Simulated factory results using Factory Explorer®

Dynamic Model Example: Dedicated vs. Flexible Testers

The anticipated advantages of dedicated test cells, as described by the Semiconductor Test Consortium, involve issues that are best examined by a discrete-event simulation software package like Factory Explorer®. The basic parameters of this example study are listed below:

- 6 products
- 3 product families
- 3 routes
- Scenario 1
  - Single tester platform for all products
  - Includes setup to switch between products
- Scenario 2
  - Tester dedicated to each product family
  - No setup needed

Note: The release rate is very low at about 1 lot/day total.

Observations

The sample model was run with the above listed data and assumptions with the following results:

- Dedicated test cells
  - Capacity loading ranged from 21% to 67%
  - Capital cost of $3M
  - Average cycle time of 2.5 days

- Flexible test cells
  - Capacity loading was 73%
  - Capital cost of $2.2M
  - Average cycle time of 2.6 days
- Both scenarios assumed identical reliability of testers
  - If open architecture provides for more predictable availability (i.e., longer MTBF, shorter MTTR), average CT will improve.

Figure 5 shows for three dedicated testers (D1, D2, and D3) versus a group of flexible testers (F1). These results were based on setting a maximum loading of 85% for any test cell. In this case, the flexible test cell was able to maintain similar aggregate WIP and cycle time with a lower capital expenditure.

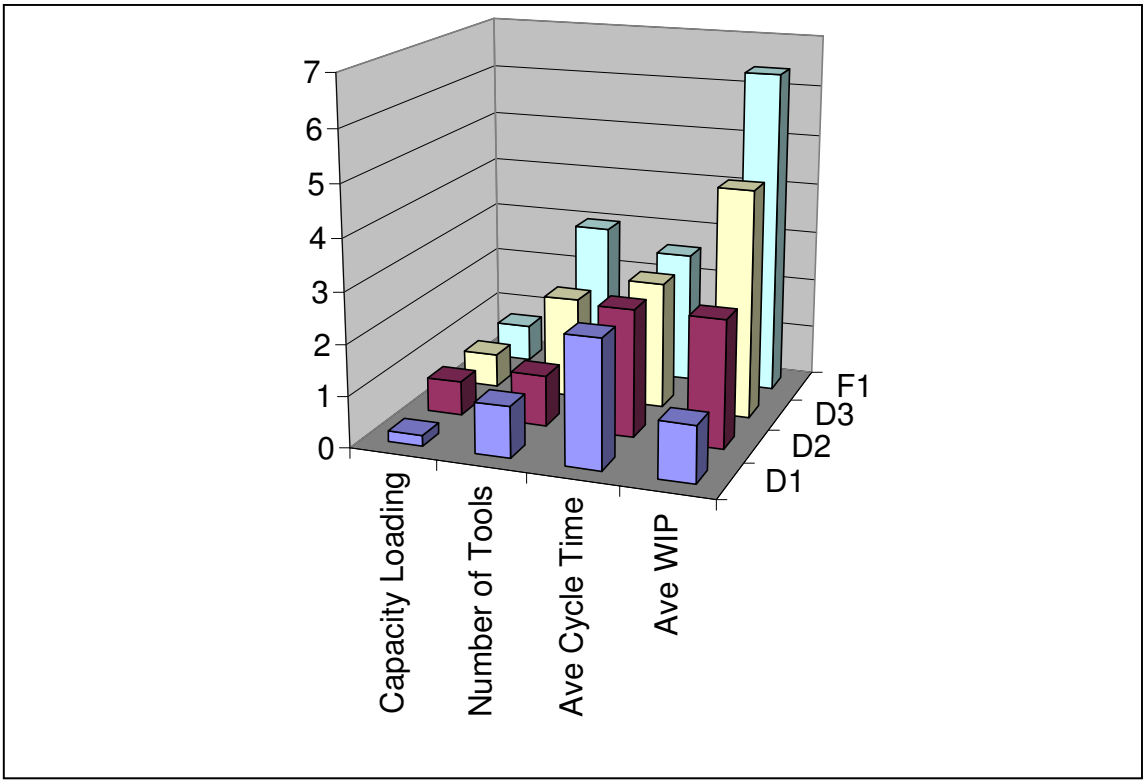


Figure 5: Simulation results where loading was maintained at a high rate

Next, the model was run by specifying the same capital budgets for both dedicated and flexible testers. This allowed the F1 test cell to operate at a lower loading. The results were a dramatic reduction in the aggregate WIP and a reduction in cycle time.

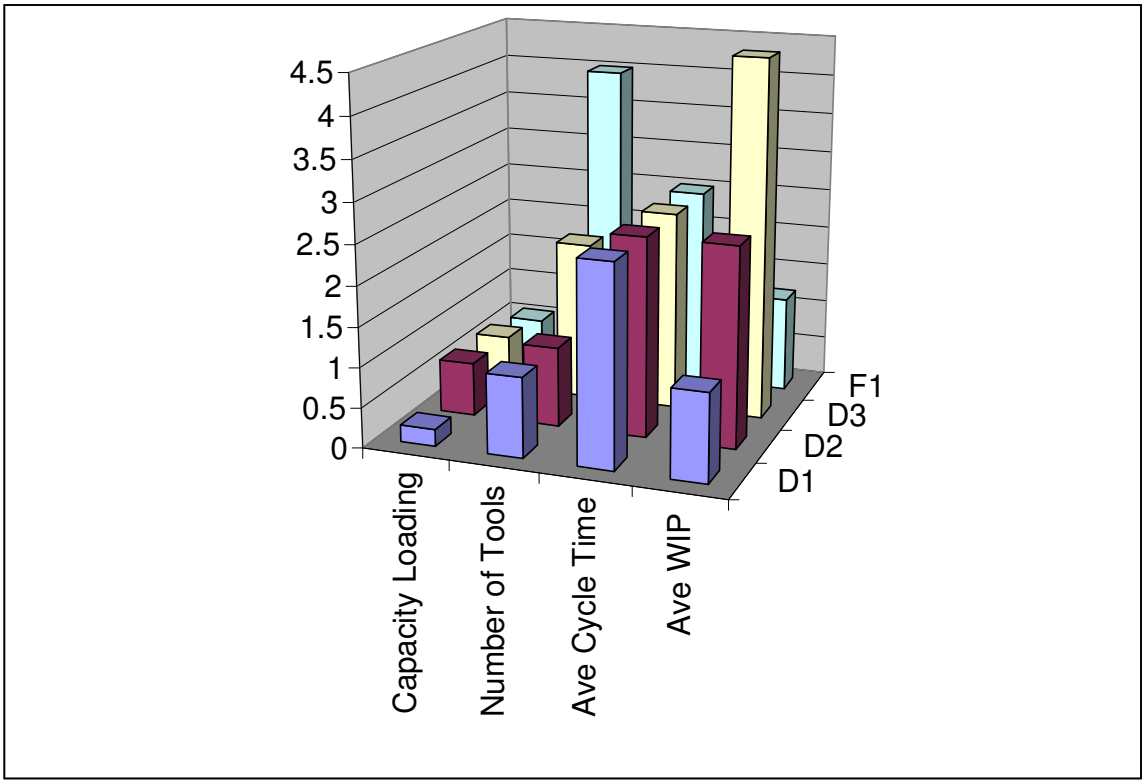


Figure 6: Simulation results with equal number of equipment

Summary

This paper has provided a review of the various modeling techniques with regards to their advantages and disadvantages for test-floor operations. We concluded that traditional cost of ownership modeling techniques are a good starting point for evaluating equipment and materials suppliers. Cell-level modeling allows for an understanding of the in-cell bottlenecks and cost drivers. Factory-level (static) modeling allows for a long-term holistic view of test-floor costs and capacity and is best applied to low-product mix, high-volume runners. Factory-level (dynamic) modeling provides a holistic approach to understanding the random nature of test-floor operations and is best applied to large-product mix with variable-run sizes.

Our preliminary dynamic modeling indicates a large potential value in moving to a more flexible, open architecture such as Global OPENSTAR™. These potential benefits include:

- Lower total capital costs
- Higher capacity loading
- Potential to improve cycle time

These benefits may be further enhanced if the predicted improvements in availability can be realized.

SEMI Needs Volunteers

The SEMI Metrics Technical Committee is looking for volunteers to participate in the next revision of SEMI E10 - Specification for Definition and Measurement of Equipment Reliability, Availability, and Maintainability (RAM). Major changes planned include defining official multi-path cluster tool RAM metrics. The next meeting of the E10 Revision Task force is planned for 8:00 AM, 11 July 2006, at the San Francisco Marriott as part of the SEMI Standards Meetings at SEMICON West. For additional information, please visit:

http://wps2a.semi.org/wps/portal/_pagr/118/_pa.118/123?dFormat=application/msword&docName=P037853

WWK to Present at 3rd Annual ISMI Symposium on Manufacturing Effectiveness

October 9-11, 2006
Hilton Austin Airport
Austin, Texas

Make your plans to attend to hear WWK's latest collaborative effort, "CMP Productivity Improvement Using Pad Surface Management." This paper is done in conjunction with TBW Industries.

The third annual International SEMATECH Manufacturing Initiative (ISMI) Symposium on Manufacturing Effectiveness will share information and methodologies for reducing manufacturing expenses in both existing and next-generation fabs through advances in equipment, process, resources, fab design, and manufacturing methods.

Challenges will be addressed in several parallel sessions dealing with fab and equipment productivity, environmental safety & health (ESH), fab design, defect inspection, statistical methods, modeling and simulation, and e-manufacturing.

The Symposium will offer papers from selected ISMI projects and leading device and equipment manufacturers. Also planned is a discussion by industry experts on the status of 450 mm wafer conversion.

WWK Hosts Cost of Ownership Seminar at SEMICON West

WWK and SEMI Co-Sponsor Event for the 14th Consecutive Year

June 13, 2006 (Pleasanton, CA) –Wright Williams & Kelly, Inc. (WWK), the world's preeminent cost of ownership software and consulting services company, announced today that it will be presenting its highly acclaimed seminar, "Understanding and Using Cost of Ownership," during SEMICON West. "Understanding and Using Cost of Ownership" will be held at the San Francisco Marriott on Thursday, July 13 from 9am to 5pm. This seminar covers all aspects of Cost of Ownership (COO) and Overall Equipment Efficiency (OEE) from fundamentals to hands-on applications. Registration for this seminar can be done directly on the Semiconductor Equipment and Materials International (SEMI) web site at www.semi.org or by calling WWK directly.

There is limited seating available for this seminar, so please contact SEMI or WWK today to guarantee your place in this once-a-year event. It is expected that registration will close out shortly for this program. As an added benefit, WWK's software maintenance clients qualify for a 20% discount off the list price of the seminar if they book directly with WWK.

With more than 3,000 users worldwide, Wright Williams & Kelly, Inc. is the largest privately held operational cost management company serving technology-dependent and technology-driven companies. WWK maintains long-term relationships with prominent industry resources including International SEMATECH, SELETE, Semiconductor Equipment and Materials International (SEMI), and national labs and universities. Its client base includes most of the top 20 semiconductor manufacturers and equipment and materials suppliers as well as leaders in nano-technology, MEMS, thin film record heads, magnetic media, flat panel displays, and solar panels.

In addition to its professional consulting and market research services, WWK's product line includes TWO COOL® for detailed process step level cost of ownership (COO) and overall equipment efficiency (OEE), PRO COOL® for process flow and test cell costing, Factory Commander® for full factory capacity analysis and activity based costing, and Factory Explorer® for cycle time reduction and WIP planning. Additionally, WWK offers a highly flexible product management software package that helps sales forces eliminate errors in product configuration and quotation processes.

ISSN 1094-9739