Information Exchange For Your Application & Use of Cost Modeling

APPLIED Co$t MODELING

Volume 12. Issue 2

Inside

Winter 2006

ISSN 1094-9739

How to Improve Fab Productivity

Carl Fiorletta
Adventa Control Technology

A popular topic for discussion in the semiconductor industry concerns fab productivity and the need to move to a 450-mm wafer size to achieve acceptable wafer fab productivity.

This idea makes me somewhat tense simply because, as we migrate to larger wafers, we take some bad habits with us – bad habits in the form of inefficient manufacturing practices. Inefficiencies at the 150 and 200-mm wafer size get extremely wasteful at 300 and 450-mm. The move to a 450-mm wafer size also raises a logical question, "when will the industry reach production quantities of 450-mm wafers, and how much retooling will be required to grow, pull, slice and polish this size wafer?"

Setting aside these raw-wafer issues, let's talk about the components of fab productivity. In its simplest form, fab productivity is the measure of revenue die produced per fab per hour. The number of revenue die produced per fab per hour must take into account a lot of productivity components.

For example, how much does a fab-hour cost? Are there opportunities for significant improvements in fab productivity that are independent of wafer size? In the following graphic, direct and indirect costs are listed:

[Continued on Page 3]

Editorial Board

Publisher

Published quarterly by:

Wright Williams & Kelly, Inc.
6200 Stoneridge Mall Road
3rd Floor
Pleasanton, CA 94588

Phone 925-399-6246
Fax 925-396-6174
E-mail support@wwk.com

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Calendar of Events

March 2006

6-8 **Global OPENSTAR® Conference**
Monterey, CA

21-23 **SEMICON China**
Shanghai, China

28-30 **FPD China**
Shanghai, China

April 2006

21-23 **SEMICON Europa**
Munich, Germany

24-26 **Strategic Business Conference**
Napa Valley, CA

May 2006

9-11 **SEMICON Singapore**
Singapore

20-24 **IIE Annual Conference & Exposition**
Orlando, FL

22-24 **ASMC**
Boston, MA

June 2006

14-16 **FPD Taiwan**
Taipei, Taiwan

July 2006

11-13 **SEMICON West (WWK booth #6648)**
Moscone Hall South, San Francisco, CA

13 **Understanding & Using Cost of Ownership**
Marriott Hotel, San Francisco, CA

Fab Productivity Measurement

Fixed costs

1. Real estate
2. Facilities
3. Taxes
4. Plant and equipment depreciation

Variable costs

1. Raw wafer cost
2. Consumables
3. Labor:
   a. Operators
   b. Process engineering support
   c. Equipment engineering and maintenance
4. Equipment:
   a. Equipment/production-hours per year
   b. Maintenance cost
   c. Operating cost
5. Utilities

The obvious productivity targets are the variable costs. Figure 1 is a listing of many cost reduction targets and how to address them.

The objective is very simple:

- Only process wafers that are revenue wafers; the processing of test and scrap or monitor wafers should not be permitted.
- Use consumables on revenue wafers only, again, no test, scrap or monitor wafers.
- Use automation technology to tune processes to keep equipment in spec, on line and producing revenue wafers.
- Use automation technology to collect data and automate process optimization to minimize hands-on, process tweaking by process engineers and operators.
- Take equipment off-line for maintenance only when recipes cannot be tuned to keep the equipment within specification.

Here are some examples of lost productivity. Based on your fab costs and production rates; you may fill in some of these blanks. In the text that follows, we'll help you derive some numbers to plug into your fab model.

Lost Productivity Examples

1. A scrapped wafer may cost ___% in lost production and $_____ in wafer cost plus the amount of value-added processing up to the point of scrapping the wafer.
2. Keeping equipment on line longer may increase production capacity by ___%.
3. Process engineering and equipment maintenance personnel may cost $____ per year.
4. Taking equipment down for maintenance based on time or cycles instead of the equipment's ability to meet spec, typically costs $_____ per year (or ____ equipment-hours per year) in lost capacity.

Our ROI worksheets comprehend these costs and help roll up the net gains in fab productivity improvement.

Using some real-world examples and case studies, here is some data that will give you guidelines to easily achievable productivity improvement. Let's look at these by process and equipment; then we'll look at fab-level productivity gains later in this article.

In Figure 2 you see what kinds of productivity gains can be achieved with run-to-run control at the equipment level. This can translate to significant productivity gains at the wafer/die and fab levels. You will see in Figure 3, Fab #2 achieves a

ISSN 1094-9739

Figure 1: Productivity Targets: Variable Costs		
Target	**What can be done**	**How to do it**
1. Raw wafer cost	Eliminate wafer scrappage	a. better process control b. eliminate operator error
2. Consumables	Minimize the number of wafers processed for a given production demand.	a. better process control b. eliminate operator error
3a Labor, operators	Assign more tools to each operator.	Automate: a. machine selection b. automate the lot move transaction at the tool c. automate process step confirmation. d. Automate the recipe download e. automate the data collection at the tool.
3b Labor, process engineering support	Reduce the process engineering sustaining effort	Automate: a. process data collection b. process recipe optimization c. recipe downloads to the tool. d. engineering change notice on production recipes. e. model-based tuning of process recipes and parameters.
3c Labor, equipment engineering & maintenance	Reduce downtime for maintenance, reduce equipment re-quals	Automate: a. process data collection b. process tuning to keep equipment within spec c. feed forward-feed backward, process data to other tools.
4a. Equipment Productivity	Increase production/hours per year	Automatically tune and optimize recipes to keep the tool on line and operating within spec.
4b Equipment Productivity	Reduce Maintenance cost	Perform maintenance when the tool can no longer be 'tuned' to run within spec. Eliminate maintenance based solely on time or cycles.
4c Equipment Productivity	Reduce Process re-qual cycles per year	By reducing the number of maintenance cycles per year, machine time lost to re-quals is reduced.

productivity gain of $23.41 million per year at the wafer/die level and $117 million per year in fab productivity gain measured in packaged die. In Fab #3, we have provided some real-world examples so that you can examine your fab data to calculate the fab productivity gains that you can achieve.

Fab Level Productivity Improvement

Now that we see what's possible at the equipment level, let's look at fab level productivity improvement.

Figure 2: Improvements at the Equipment Level using Run-to-Run Control

CMP on Strasbaugh tool:

Sigma	-55%	Fewer lookaheads
Mean centering	+85%	Automatic SPC (24/7) with forced tool shutdown.
Cpk	+100%	
Rework	-10%	Less operator influence
Scrap	-8%	Real deterministic data

Ion Milling, tool: Veeco

Sigma	-40%	Fewer lookaheads
Mean centering	+15%	Reduced number of recipes
Cpk	+50%	Automatic SPC (24/7) with forced tool shutdown.
Scrap	-5%	Less operator influence
		Real deterministic data

Litho Overlay Control tools: Canon tool I4/I5 Deep UV Stepper, KLA 5100 Metrology, FSI litho cell, with ASML Stepper

(Here we use model-based control to calculate overlay parameters based on previous lot measurements on a run-to-run basis.)

Fab capital avoidance	$20 million
Rework reduction	75%
Cpk improvement	+40%
Probe yield improvement	+4 to 6%
Process engineering effort	-50%

Automatically control:
X & Y markshift
X & Y scaling
Magnification

Automatically adjust: 15,000 controller parameters

Gate Etch, tool: Applied 5200

(Here we use model-based control to calculate etch time)

Identified major sources of process variation:
Photo process, stepper to stepper variation
Etch, device-to-device variation
Cpk improvement 2.04 to 3.44
Eliminate 8 hrs cycle time per lot via reduced test wafers

Single control strategy:
etchers, 3 targets, 200,000 parameters (steppers) x (etchers) x (reticles

CMP tool: Applied Mirra

(Here we use run-to-run control to control polish time. The goals included increasing Cpk, decreasing test/pilot wafers and decreasing rework)

Fab capital avoidance	$36M
Equipment thruput	+25%
Wafer rework	-7%
Scrap Reduction	40%
Cpk improvement	150%
Test wafer reduction	40%

CMP, tool: Strasbaugh

Sigma	-55%	Fewer lookaheads
Mean centering	+85%	Automatic SPC (24/7) with forced tool shutdown
Cpk	+100%	
Rework	-10%	Less operator influence
Scrap	-8%	Real deterministic data

With the equipment productivity improvement as a basis for what can be achieved at the equipment level, let's roll this up to the fab level to see what the overall improvements in fab productivity might be.

Your Mileage May Vary

Summarizing the equipment and fab level productivity gains shown in Figures 2 and 3, here are some numbers that you can plug into your fab model to calculate the improvements that you may expect from a fab level implementation of run-to-run control.

Fab Model for Productivity Improvements

- Average Cpk improvement 85%
- Scrap reduction 10 to 40%
- Test wafer reduction 35 to 45%
- Average capacity increase 12%

Figure 3: Fab Level Productivity Improvement using Run-to-Run Control

Fab #1: Wafer starts: 17,500/month

Tools managed by run-to-run/model-based process control

Improvements with run-to-run control

12% fab level capacity increase

25% increase in tool productivity:

-includes reduction in test, monitor and test wafers

2%increase in probe yield

-via improved process control and reduced process variability

Fab #2: 45,000 wafers/month

Improvements with run-to-run control

Fab capacity increase	12%
Revenue Increase for the fab (wafer die)	$23.41 million
Revenue Increase for the fab (packaged die)	$117 million

Fab #3:

Improvements with run-to-run control

Fab capacity increase	20%
Increase in machine hours/year	25%
Reduce Test and Scrap Wafers	90%
Reduction in rework	96%
Increase yield	3-10%

Additional Value to the Fab

Reduce process engineering Time

Reduce Capital Equipment Requirements

$20M in litho

$36M in CMP

Increase in Revenue and Profit.

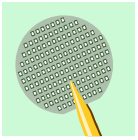
These numbers depend on annual

Volume and value per wafer or packaged die.

Looking Ahead

As we think about the next wafer size, it is important to consider the manufacturing inefficiencies that pervade our industry. While semiconductor manufacturing may be the only discipline that consciously accepts the manufacture and processing of material to be scrapped – consuming expensive materials and valuable fab process time – we should plan for a time when all wafers are revenue wafers; process control is more automated and equipment monitoring is completely automated, with less intervention by equipment and process engineers as well as operators. As we fully embrace 300-mm manufacturing and migrate to the next wafer size, wouldn't it be practical to leave our bad habits behind? They cost us a lot of time and money.

We've come a long way, from 25-mm to 300-mm wafer size, with serious consideration of 450-mm wafers. This is a good time to think about changing the way we manufacturer semiconductor devices from two points of view; wafer size and wafer processes. As we see from the above data, there are a lot of productivity gains to be achieved simply by improving the way we operate existing factories. Beyond that we might ask, should we go forward with larger wafers, using the manufacturing techniques we have today, or should we migrate away from business as usual and towards advanced process control?



Wright Williams & Kelly, Inc. Launches Chinese Language Web Site

Web Site Recognizes the Importance of Manufacturing in Native Chinese Speaking Regions

February 8, 2006 (Pleasanton, CA) – Wright Williams & Kelly, Inc. (WWK), a cost & productivity management software and consulting services company, announced today the launch of its new web site which includes both Traditional and Simplified Chinese language translations. The addition of both languages is in recognition of the key role that Mainland China, Taiwan, and Hong Kong are playing in high tech manufacturing.

"This latest addition to our web presence, which is now over a decade old, is very exciting", stated David Jimenez, WWK's President. "The center of gravity in high tech manufacturing is leaning towards Southeast Asia and the powerful influence of China and Taiwan. Providing the content of WWK's English language web site in both Traditional and Simplified Chinese is the next step in upgrading our support for that region of the world."

ISSN 1094-9739

International Technology Roadmap for Semiconductors 2005: Cost and Economics

WWK Software ties to ITRS Challenges

By Daren Dance, VP Technology, Wright Williams & Kelly, Inc.

Since its inception as the National Technology Roadmap for Semiconductors, the International Technology Roadmap for Semiconductors (ITRS) has provided guidance to all involved with semiconductors, materials, and equipment. In this role, the ITRS has consistently identified opportunities for using cost and economic modeling to improve processes, products, and equipment. Quoting the 1997 roadmap, "The ability to reduce the cost per function by an average of 25 – 30% each year represents one of the unique features of the semiconductor industry."[1] That challenge or "unique feature" of the semiconductor industry remains – the need for cost modeling and simulation continues.

The ITRS is founded on this economic assumption:

> Since its inception in 1992, a basic premise of the Roadmap has been that continued scaling of microelectronics would further *reduce the cost per function* . . . Thus, the Roadmap has been put together in the spirit of a challenge—essentially, "What technical capabilities need to be developed for the industry to stay on Moore's Law . . .?"[2]

We will not try to summarize each of the identified challenges, but Table 1 briefly lists some of the grand (or overall) challenges. These are divided into near-term and longer-term challenges, showing both performance-enhancement challenges and cost-effective manufacturing challenges.

The performance-enhancement and cost-effective manufacturing challenges in Table 1 are highly interdependent. For example, the performance-enhancement challenge of power consumption drives the cost-effective manufacturing challenge of packaging costs.

Figure 1 summarizes some of the more importance near-term performance-enhancement / cost-effective manufacturing relationships. Notice that almost every one of the performance challenges has a significant cost interaction – either manufacturing or packaging cost. Further, since the major reason to scale to 32-nm is the continuation of Moore's economic law, we did not include that interaction in Figure 1.

The ITRS uses two examples of Moore's Law cost per function to trend economic progress:

- For DRAM and other memory chips, the Moore's Law trend follows cost per memory bit.
- For MPU's and logic circuits, the Moore's Law trend follows cost per transistor.

The 2005 ITRS forecasts for these metrics are shown in Figure 2. Similar forecasts for packaging and assembly costs are shown in Figure 3. This figure shows assembly and packaging cost per pin for two types of products – Cost/Performance products (such as high performance

[1] *The National Technology Roadmap for Semiconductors: 1997 Edition*, L. Wilson Ed., Semiconductor Industry Association, San Jose, Ca.

[2] "Executive Summary," *International Technology Roadmap for Semiconductors: 2005 Edition*, p. 1, italics added.

microprocessors) and Low Cost/Hand Held products. Since assembly and packaging costs vary significantly depending on the actual device being assembled, the bars in Figure 3 show the range of estimates.

Table 1: 2005 ITRS Grand Challenges

Near Term Challenges (2005 – 2013)	Longer Term Challenges (2014 – 2020)
Performance-Enhancement - Scaling to 32-nm - Signal isolation - High-performance, low-cost RF and mixed signal - New gate stacks and materials - Lithography (Immersion & EUVL) - Critical dimension control - Interconnect manufacturability - Power consumption - Front end processes	Performance-Enhancement - Advanced, nonclassical CMOS devices - Statistical process variation - CD and process control - Global interconnect - Leakage and power consumption
Cost-Effective Manufacturing - Design productivity - Test of complex devices - Responding to rapidly changing business requirements - Trade-off between manufacturing cost and cycle time - Packaging cost - ESH assessments of new materials - Signal-to-noise ratio - Metrology, inspection, and diagnosis - Measurement of complex stacks	Cost-Effective Manufacturing - Design for manufacturability - Next generation starting materials (450-mm wafers) - ESH design for chemical and material management - Process stability and contamination - In-line defect analysis - Nondestructive process measurements - New materials modeling

Figure 1: Interdependence of near-term grand challenges[3]

Performance Challenges

	Design productivity	Test of complex devices	Rapidly changing business requirements	Cost and cycle time trade-off	Packaging cost	ESH assessments of new materials	Signal-to-noise ratio	Metrology, inspection, and diagnosis	Measurement of complex stacks
Scaling to 32nm	X	X						X	X
Signal isolation					X		X		
RF and mixed signal	X	X			X		X		
New gate stacks and materials			X			X		X	X
Lithography (Immersion & EUVL)	X			X		X		X	
Critical dimension control	X			X				X	X
Interconnect manufacturability				X			X	X	X
Power consumption		X			X		X	X	
Front end processes				X		X		X	X

Cost Effective Manufacturing Challenges

[3] Not all possible challenge interactions are noted in Figure 1 – We limited each performance challenge to 4 important cost effective manufacturing challenges.

Figure 2: ITRS Forecasts of Economic Trends[4]

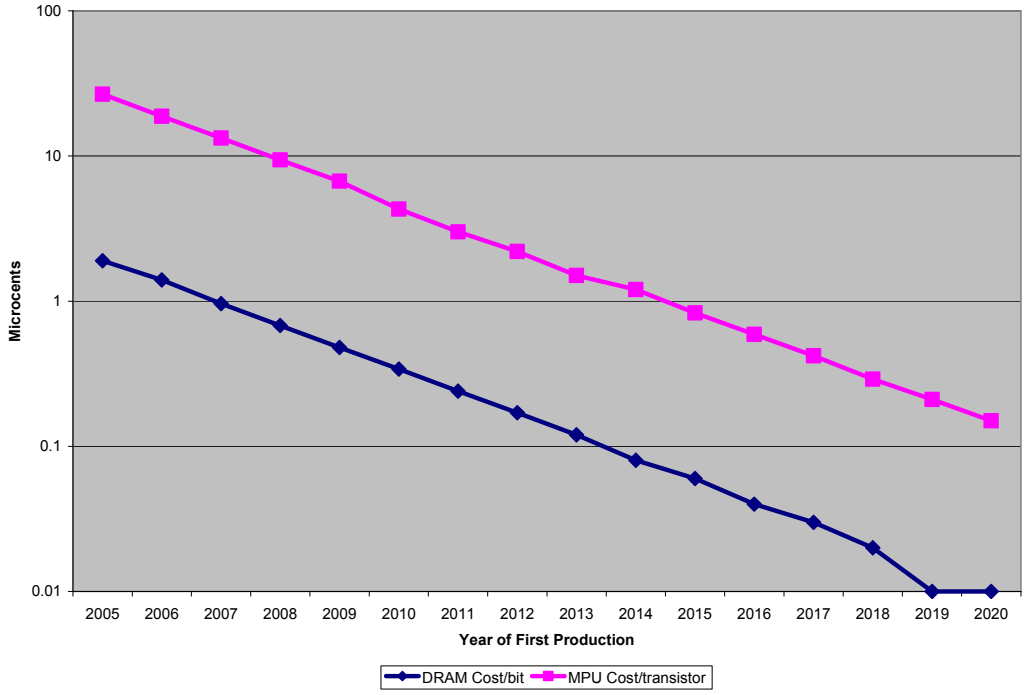
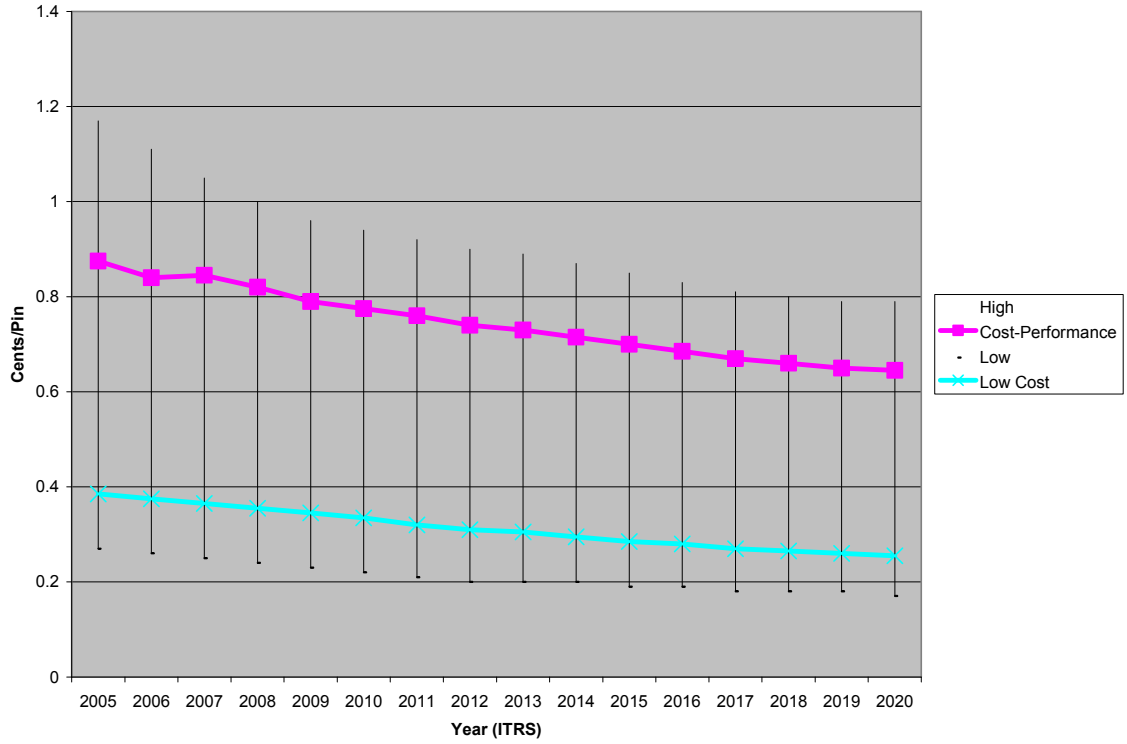


Figure 3: Assembly/Packaging Cost Trends[5]



[4] 2005 ITRS, "Overall Roadmap Technology Characteristics", Tables 7a and 7b, p. 84.
[5] 2005 ITRS, "Overall Roadmap Technology Characteristics", Tables 4a and 4b, p. 78.

The success of the semiconductor industry in addressing Moore's Law has resulted in changes to the structure of the 2005 ITRS. Note the following quote from the 2005 Executive Summary:

> The 2005 ITRS represents a major departure from the previous versions of Roadmaps because it removes the concept of "technology node" as the main pace setter for the IC industry. In the past, DRAM products set the technology pace by quadrupling the number of bits every three years with the introduction of a new major technology generation. . . However, the increase in the number of bits by four times from one technology node to the next led to a continuous increase in die size that eventually negatively affected the economics of this silicon cycle. In an attempt to minimize the increase in die size many IC companies accelerated the speed at which new technology nodes were introduced . . . [6]

As a result, the 2005 ITRS now focuses on year of first production, as illustrated in Figures 2 and 3, rather than DRAM half-pitch and technology nodes. This change, however, does not change the overall cost challenges that the industry faces. Table 2 lists the cost and economic challenges that WWK has extracted from the ITRS technology working group summaries.

Table 2: Cost Challenges from Working Group Summaries[7]

Technology Working Group	Difficult Challenges Related to Cost
Design	• Cost-driven design flow
Test and Test Equipment	• Continued economic scaling of test including the trade-off between cost of test and test quality • Costs for interface hardware and test sockets
Process Integration, Devices, and Structures	• Implementation of high-κ dielectric and metal gate electrode
RF and Analog Mixed-Signal Technologies	• Cost and integration complexity of integrating bipolar devices in aggressively scaled CMOS • Cost and performance trade-offs associated with integrating passive devices in scaled CMOS
Emerging Research Devices	• Development of a manufacturable, cost-effective fabrication technology integratible with the CMOS logic process flow
Front End Processes	• Economics of the incumbent Czochralski crystal pulling, wafer slicing, and polishing processes are questionable beyond 300-mm
Lithography	• Achieving constant/improved ratio of exposure-related tool cost to throughput over time • Cost-effective resolution-enhanced optical masks and post-optical masks • Reducing mask data volume • ROI for small volume products • Achieving ROI for industry with sufficient lifetimes for exposure tool technologies
Factory Integration	• Reduced time to ramp factories, products, and processes to stay competitive with rapidly changing business environments • Ability to constantly adjust equipment loading to keep the factory profitable • High cost and cycle time of mask sets for manufacturers impacting affordability of new product designs • Understanding up-front costs to incorporate extendibility, flexibility, and scalability

[6] 2005 ITRS, "Executive Summary," p. 1.
[7] Extracted from 2005 ITRS, "What is New for 2005 – The Working Group Summaries", pp. 22-53.

Assembly and Packaging	• Low-cost embedded passives • Increased wireability at low-cost • Conformal, low-cost organic substrates • Handling in low-cost operations • The partitioning of system designs and manufacturing across numerous companies will make optimization for performance, reliability, and cost of complex systems very difficult
Environment, Safety, and Health	• Need for innovative energy- and water-efficient processes and equipment • Need for efficient thermal management of cleanrooms and facilities systems • Need for more efficient utilization of chemicals and materials, and increased reuse and recycling
Yield Enhancement	• Detection of multiple killer defect types is necessary at high capture rates, low cost of ownership, and high throughput • Need for high-speed and cost-effective high aspect ratio inspection

WWK provides a comprehensive suite of operational modeling solutions ranging from focused process to high level factory analysis tools. These tools are useful in meeting the cost challenges identified by the ITRS. Some of the applications for these tools include:

- Upgrading factories
- Building new factories
- Designing new process and equipment
- Extending equipment designs to new technologies and retrofitting existing tools
- Developing new materials and new applications for existing materials

Using cost modeling and simulation will foster decisions that reduce risk and increase return on investment. Table 3 indicates how WWK can address some of the issues identified by the 2005 ITRS.

Table 3: WWK Applications for ITRS Issues[8]

	TWO COOL® PRO COOL ®	**Factory Commander®**	**Factory Explorer®**	**COOL FUSION™**
	Cost of Ownership	Factory Level Cost and Resource Model	Capacity, Cost, and Simulation Analysis	Sales Support
Design		Cost analysis of design flows and methods	Simulation of design productivity	
Test and Test Equipment	COO for Test and Metrology	Estimate the impact of test on factory costs	Impact of test – including yield – on factory operations	COO support for test equipment and services
Process Integration Devices, and Structures	Process equipment and process flow COO	Product cost	Capacity/cost analysis and optimization	
RF and Analog	Process equipment	Product cost	Capacity/cost	

[8] Also see "The National Technology Roadmap for Semiconductors: Applications of Cost Modeling", 1997, www.wwk.com

Mixed-Signal Technologies	and process flow COO		analysis and optimization	
Emerging Research Devices	New equipment COO	New process and integration	Capacity/cost analysis and optimization	COO support for new equipment and services
Front End Processes	Equipment COO	Impact of material on manufacturing cost	Material impact on overall supply chain	COO support for new equipment and services
Lithography	Mask and process equipment COO	Estimate the litho and mask impact on factory costs	Capacity/cost analysis and optimization	COO support for new equipment and services
Factory Integration		Product cost and impact of new tool on factory costs	Factory scaling and capacity/cost analysis	
Assembly and Packaging	Equipment COO	Integrating wafer fab and assembly costs	Overall supply chain capacity/cost analysis	COO support for new equipment and services
ESH	ESH impact on COO	Benefits of reuse/recycling	Overall supply chain ESH impact analysis	COO support for new equipment and services
Yield Enhancement	Equipment and material COO/ROI	Yield impact on factory costs	Capacity, costs, and benefit analysis	COO support for new equipment and services

Free Software Development Cost Estimator COOLSoft™ v2.0 Available as Web Download

January 12, 2006 (Pleasanton, CA) – Wright Williams & Kelly, Inc. (WWK), a cost & productivity management software and consulting services company, announced today the availability of COOLSoft™ v2.0, its latest generation software development cost estimating tool. COOLSoft™ utilizes a hybrid approach of intermediate and detailed versions of the Constructive Cost Model (COCOMO). This allows for the reuse of existing code, development of new code, the purchase and integration of third party code, and hardware integration. The output is then displayed as man-months of programming effort, calendar schedule, support costs, and hardware costs.

"We have used COOLSoft™ for the past decade as an internal guide to our development projects," stated David Jimenez, WWK's President. "This latest release transforms our internal tools into a commercial grade application that any organization involved in software development or maintenance will see as a great benefit. Software development budgets and timelines are always met with skepticism by management and COOLSoft™ provides a quantitative approach to help reduce uncertainties."

COOLSoft™ download instructions are available on the WWK web site by selecting the Products link and then the COOLSoft™ link.

ISSN 1094-9739

Michael Wright Joins Wright Williams & Kelly, Inc. Board of Directors

Former Entegris (NASDAQ: ENTG) President and Current Advisor to the CEO Strengthens WWK's Strategic Direction

February 2, 2006 (Pleasanton, CA) – Wright Williams & Kelly, Inc. (WWK), a cost & productivity management software and consulting services company, announced today the election of Michael W. Wright as outside director. This appointment further solidifies WWK's strategic direction as the world's preeminent cost modeling resource.

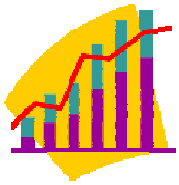
Michael Wright's career is a rare blend of deep knowledge and clarity of vision acquired through multiple leadership roles in semiconductor and related technical industries. He is the former President and COO of Entegris, the acknowledged global leader in materials integrity management. Through Wright's efforts, Entegris grew from $260 million in revenue to $700 million in 2005. Michael has contributed corporate leadership in a broad range of executive management positions at such flagship technology companies as Integrated Air Systems (IAS), General Signal (GCA, Ultratech), IDC, Integrated Solutions and Empak.

During his close association with SEMATECH, he founded Wright Williams & Kelly, Inc. (WWK), which today has become the largest privately-owned provider of cost-of-ownership software and operational cost modeling tools for the semiconductor and other technology-intensive industries. He is an experienced international executive who, over the last two decades, has built relationships, joint ventures, partnerships and facilities from Asia to Eastern Europe.

Michael recently co-authored the book, "The New Business Normal", an acclaimed exploration of the perspectives and practices required for business vitality in the accelerated, globalized conditions of our new century. Currently he serves as senior advisor to the CEO at Entegris, is on the board of August Technologies (NASDAQ: AUGT), Starview Technologies and the Minnesota High Technology Association (MHTA).

"I am pleased to accept this appointment," stated Michael Wright, "and look forward to assisting WWK in formulating its next generation strategic vision to address the needs of its expanding market presence. I am confident that their cost management expertise and software solutions will provide great benefit to any industry seeking to improve its gross margins."

"We are pleased to have Michael rejoin the organization on a more active basis," stated David W. Jimenez, WWK President and Chairman. "Michael's proven leadership and broad industrial networking will help lead WWK into the next phase of our aggressive growth. His expertise in developing a world class marketing strategy will be highly leveraged at WWK and he was recently recognized through the EXCEL Minnesota award for his significant role in nearly tripling the revenues of Entegris in the last five years."



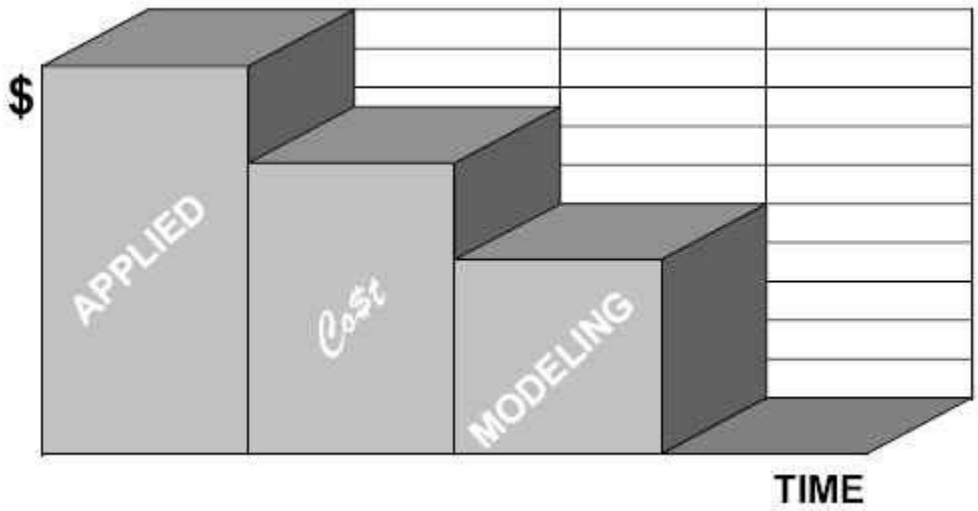
SEMI Award for North America: Nominations are Now Being Accepted

Each year, SEMI publicly recognizes and honors technological and industrial leadership through the SEMI Award North America program. The awards program was established in 1979 to recognize enabling technical contributions by individuals and teams to the microelectronics industry. The enabling technological contributions to the microelectronics industry can be as broad as Integrated Circuit Design, Design for Manufacturability (DFM), new mask manufacturing methods, new device manufacturing architecture and methods, and the assembly and test of integrated circuits and microelectromechanical (MEMS) devices.

Submit your nominations for this prestigious award now. We'd like to know who you feel is deserving of the SEMI Award for North America. The awardee can either be the originator of a concept, material, process, equipment, factory operation innovation or one who has made significant enhancements or additions to a concept which enabled its successful implementation in the commercial market. If you know of someone or a team of people who have made a significant contribution to the semiconductor industry and should be nominated for the 2006 award, simply complete the form at the link below

http://dom.semi.org/web/Wevals.nsf/SEMIAward?OpenForm

Your nomination will be reviewed and selected by the SEMI Award for North America committee. Nominations for the 2006 SEMI Award for North America must be submitted by **May 12, 2006** to be considered.



ISSN 1094-9739