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Inside

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When Capacity Buys are not an Option: Technical Trends in c-Si Cell Manufacturing and their Implications

With this edition of Applied Cost Modeling, we are publishing the first installment in a series examining the business considerations associated with the adoption of new processes, equipment, or materials for crystal silicon-based (c-Si) photovoltaic (PV) cell manufacturing.

Introduction

Economics will always play a crucial role in the way photovoltaic (PV) technology advances. However, the current generation of products is facing substantial business challenges in the attempt to scale their technologies. This paper is the fifth in a series covering business analysis for PV processes. The methods applied in these papers fall into two categories, cost of ownership (COO) and cost and resource modeling. Both methods examine the business considerations associated with the adoption of new processes, equipment, or materials. This is more critical than ever. Near term issues, in some cases the survival of the business, heavily influence today's decision processes. We have tried to identify the areas we think will produce the largest near term paybacks. The areas we have identified are n-type wafers, Al_2O_3 passivation, and copper metallization.

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Calendar of Events

September 2013

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Parc des Expositions
Paris, France

October 2013

1-4 **EU PVSEC**
Parc des Expositions
Paris, France

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Messe Dresden
Dresden, Germany

21-24 **Solar Power International**
McCormick Place
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28-31 **North American Standards Meeting**
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10-13 **International Technology Partners**
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December 2013

4-6 **SEMICON Japan**
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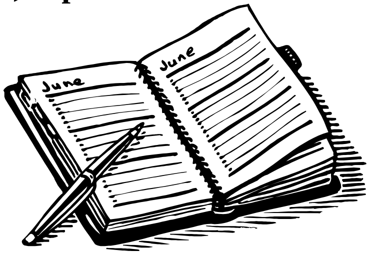
Chiba, Japan



Solar Cell Production Outlined

Any discussion of technical changes to any steps in crystal silicon (c-Si) PV manufacturing must take into consideration the entire solar cell production flow. So before we describe the processes of interest it is worth first outlining the baseline process through which the silicon wafer travels on its way to becoming a fully-fledged solar cell.

The silicon wafer is sliced from a monocrystalline or multicrystalline silicon ingot. This step can be carried out either directly at the silicon foundry or by the solar cell manufacturer. The sliced wafer then goes through several distinct manufacturing steps after which it is ready for mounting into a solar panel.

The first step in the cell manufacturing cycle is wet etching, which is described in depth in the second paper in this series[1]. Here, the imperfections created in the sawing process are removed, after which the wafer's surface is texturized to create the microscopic pyramid structures that will enable it to trap sunlight rather than reflecting it.

Described in the first paper in this series[2], the second step is a thermal diffusion process whereby an n-type layer is diffused through the wafer's top layer and down into its structure. Typically made of phosphorous-rich material, this combines with the wafer's own p-type material to create the cell's p/n junction, a planar semiconductor device that will generate electrical current. During the diffusion process, a layer of glass is created on the surface of the cell that is removed in an additional etching and deglassing process.

In the third step, the cell's antireflective (AR) layer, is laid down in a plasma enhanced chemical vapor deposition (PECVD) process that gives the cell its blue color, after which the cell is ready for metallization. This was described in detail in the third paper in this series[3]. The PV industry uses screen printing as the method of choice for depositing silver and aluminum onto its solar cells.

Market Trends

Solar PV equipment spending was US$3.6 billion for 2012 down from US$12.9 billion in 2011, according to new research in the latest NPD Solarbuzz PV Equipment Quarterly report. Covering c-Si ingot-to-module and thin-film, the report says spending for 2013 could drop to levels not seen in the industry since 2006. “Spending for 2013 is forecast to decline even further to US$2.2 billion,” said Finlay Colville, Vice-President of NPD Solarbuzz. The market analyst group expects only eight PV equipment suppliers to have PV-specific revenues during 2012 in excess of US$100 million, compared to 23 in 2011.

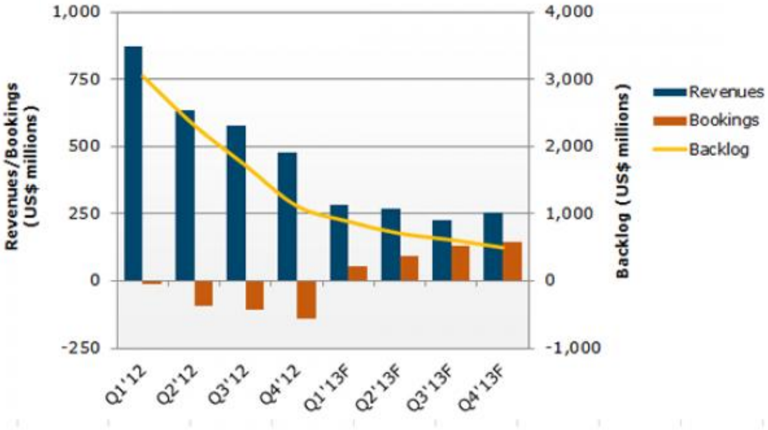


Figure 1: Forecasted PV-Specific Metrics for the Top 10 PV Equipment Suppliers (NPD Solarbuzz)

“Excessive investment in 2010 and 2011 was the catalyst of the over-capacity and over-supply situation that exists today. It was also a key factor in end-market price erosion that forced many of their customers to file for insolvency. The days of PV-specific backlogs and revenues at the billion-dollar level are unlikely to be repeated for at least three years."

With so much competitive c-Si capacity shipped during 2011 and 2012, NPD Solarbuzz states that the biggest fear for equipment suppliers is the emergence of a secondary equipment market across China and Taiwan. Most importantly, this would delay any upturn in equipment spending.

With regards to module shipments and revenues, IHS iSupply is expecting overall global installation markets to pick up again after the first six months of 2013 and then continue to improve over the course of the year. Meanwhile, overcapacity that had built up because of massive investments in 2010 and 2011 will have less dramatic repercussions in 2013 than during 2012.

The IHS report said the decline in PV module prices afflicting the market will slow down in 2013 and then eventually stop by the second half of the year. By the fourth quarter of 2013, average crystalline module prices are forecast to reach US$0.55 per watt, down 14% from the same time in 2012, compared to a bigger contraction of 32% between the fourth quarter of 2011 to 2012. Overcapacity, a decline in pricing, as well as slowing growth in key worldwide markets will serve to keep the global PV market for solar modules depressed, with recovery not expected until well into the second half of 2013. While this sounds better than the scenario for equipment suppliers, double-digit price erosion isn't something that the market can sustain indefinitely.

This is not a rosy picture for the PV market, or its supply chain, and one of the conclusions is that, for many, it may never be so again. Why? The larger macroeconomic environment has changed. To a large degree, PV remains dependent on favorable government policies (subsidies, feed-in tariffs, carbon taxes, etc.). These policies are struggling to gain (or maintain) traction as governments (e.g., U.S, Spain, Italy) struggle with massive budget deficits and accumulated debt. Separately, the widespread use of hydraulic fracturing has reduced natural gas (a competing source of electricity generation) prices by a factor of 3. Further, the natural gas supply chains are extremely well capitalized, involving some of the largest and most profitable corporations in the world.

In short, there is an oversupply of product, a substantial risk on the demand side due to financial constraints with governments, and a competitive technology (natural gas) that has undergone substantial and sustainable cost reductions.

What does this mean going forward? The bar has been raised. It is tempting to compare the solar industry with the semiconductor industry, where boom and bust cycles are common. However, the boom-bust cycles in the semiconductor industry have almost always been traced to basic supply and demand. It has been decades since it was highly dependent on government policy and most of the competition has come from within the IC industry, not from competing technologies outside the industry.

One clear reality—there is no more room for current generation "me too" PV roadmaps. Current "me too" products are unlikely to be profitable for a long time, if ever. With double digit price erosion for c-Si modules, manufacturers must look for competitive advantages and those cannot be had with older, off-the-shelf processes. Upgrading processes is the only potentially viable business plan. In practice, companies should get accustomed to continuous upgrading; a static solar cell factory will not remain competitive for long, now or at any time in the foreseeable future. Just to be clear, the market will punish those who do nothing to improve their processes. As hard as it is to invest in a down cycle, it is the only way to survive.

Does that mean the end of "turnkey factory sales?" The authors think that is a likely outcome. Additionally, we see module manufacturers acquiring unique technologies at the cell level to ensure their survival through sustainable competitive advantages. As a result, we expect to see several announcements involving a deeper level of partnering, (likely including acquisitions) of novel cell manufacturers and IP developers before their technologies have been released to the broader market.

Technology Upgrades

The question then becomes, given the current challenges, where to look for these technology developments that have the potential to create competitive advantages? In this section, we look at our best guesses for short term opportunities – those that can begin making an impact within 12 months, as well as other potential areas of interest. We conclude this section by looking at one "up and coming" approach to improvements in cell efficiency and reductions in cell manufacturing costs.

N-type wafers[4]

An early driver of PV was satellites. P-type cells (boron doped) proved to be less sensitive to degradation caused by exposure to cosmic rays than n-type cells. This early application drove p-type cell development and that is where most production remains today. Recent research suggests a likely move to n-type (phosphorus doped) cells. The results have shown a potential to outperform p-type cells in terms of efficiency. According to the International Technology Roadmap for Photovoltaics (ITRPV 03/2012), n-type cells market share could reach approximately 30 percent of the monocrystalline silicon solar module market by 2015 (currently around 5 percent).

The advantages of n-type cells is they do not suffer from light induced degradation (LID) seen by p-type cells. In addition, n-type cells are less sensitive to impurities typically present in silicon feedstock. Therefore, n-type cells with higher efficiency can theoretically be produced at a lower cost than p-type cells using the same wafer manufacturing methods (Czochralski crystal pulling). However, n-type wafers show a larger distribution of electrical resistance. This leads to a reduction in the number of wafers yielded from an ingot. One proposed solution is to use a continuous feed Czochralski puller, which would provide equipment companies with new sales opportunities.

Al_2O_3 passivation[5]

Al_2O_3 is of increasing interest due to the promise it holds to provide excellent passivation of p-type c-Si surfaces at industrial feasible scales. While Al_2O_3 exists in different crystalline forms, amorphous Al_2O_3 films are used for passivation layers. The films are transparent over the wavelength region of interest for solar cells. Al_2O_3 films for c-Si surface passivation can be deposited by atomic layer deposition (ALD), plasma-enhanced chemical vapor deposition (PECVD), as well as physical vapor deposition (PVD) sputtering. Sol-gel processes have also been investigated. Annealing of the films is typically required to achieve a high level of surface passivation. Results of Al_2O_3 with n-type cells have shown greater than 23% efficiency.

PECVD and PVD are certainly scalable in c-Si PV manufacturing. The competitive edge of existing PECVD systems is that they can easily be modified to avoid large investments in new technologies. The results reported for PVD have not been as good as for PECVD and ALD. Conventional ALD is unsuitable for high-throughput solar cell production. However, throughput can be addressed by batch processing or through spatial-ALD (based on spatial separation of precursor gasses instead of time based separation), which would allow for inline atmospheric processing.

With regards to cost, it has been reported that the deposition of Al_2O_3 can be accomplished for just a few cents per cell. However, the implementation of rear-surface passivation schemes can have a major impact on COO. One important cost related finding is that passivation using Al_2O_3 does not require a semiconductor grade precursor, but that solar grade $Al(CH_3)_3$ shows excellent results as does using less pyroforic precursors.

Cu metallization[6]

The metallization of c-Si cells is one of the main cost drivers in the manufacturing process[3]. Screen printing of silver pastes is still the dominant technique, but the need to replace silver with copper to lower costs is widely acknowledged. While elemental silver has better conductivity than elemental copper, electroplated copper has superior conductivity when compared to current silver pastes. Data indicates up to a 0.5% cell efficiency improvement with electroplated copper.

Using copper as an electrode material for c-Si cells has a number of issues that need to be addressed. First, copper diffuses into the silicon where it forms a trap for the charge carriers in the semiconductor material. Consequently, a diffusion barrier is required. Secondly, copper, unlike silver, oxidizes into a porous compound when exposed to air. Addressing this issue requires extra protection of the electrode contact, (e.g., capping). Thirdly, the use of copper as an electrode material increases the complexity of the solar cell manufacturing process. For example, in order to make contact with the silicon wafer, the silicon nitride passivation layer must be opened by either etching or laser ablation. Subsequently, a diffusion barrier must be deposited followed by copper deposition. The latter can be done by electroplating, a technique that is well known in the integrated circuit (IC) industry, albeit at throughputs far below the requirements for solar manufacturing.

Additional paths

There are many possible approaches to improved cell efficiency and, hopefully, lower manufacturing costs (cost/watt) resulting in subsequent improvement in costs for the end user (LCOE - levelized cost of electricity) and in total cost of ownership for energy (TCOe™). While the previously mentioned approaches, in the authors' opinions, have the best chances of impacting manufacturing during the next 12 months, there are other approaches that warrant mentioning.

Selective emitter[7]

The advantages of a selective emitter cell include a low contact resistance due to heavy doping underneath the metal grid, improved front-surface passivation of the lightly doped region between the grids, and reduced recombination under the metal contact. However, the very material that gives the p/n junction its functionality also forms a significant barrier to light in the blue part of the spectrum.

Selective emitters address this issue by varying the amount of phosphorus across the surface of the cell. The basic principle is to deposit more phosphorus directly under the metal grid to improve the contact between the metal and the silicon, allowing electrons to migrate more efficiently. Additionally, reducing the amount of phosphorus between the grid fingers reduces recombination losses that improve the cells blue response.

There are a number of approaches to creating selective emitters that include: doped silver paste, screen printing, selective diffusion, laser doping, etchback, doping paste etchback, buried contact, and ion implant. However, the disadvantage to any of these processes is that their improvement in blue spectrum response is attenuated by the absorption of the blue spectrum by other module components (glass and ethylene vinyl acetate - EVA). It is estimated that these materials reduce the benefit of selective emitters by 50%. Until improvements on the module end allow the full value of selective emitters to be extracted in the field, the benefit of the more costly and complex selective emitter cell processes will be mitigated.

Heterojunction with Intrinsic Thin Layer (HIT™ or HJT)[8]

In a HIT/HJT solar cell structure, an intrinsic amorphous silicon (a-Si) layer followed by a p-type a-Si layer is deposited on a randomly textured n-type c-Si wafer to form a p/n heterojunction. On the other side of the c-Si cell, intrinsic and n-type a-Si layers are deposited to obtain a Back Surface Field (BSF) structure. On both sides of the doped a-Si layers, Transparent Conducting Oxide (TCO) layers are formed and finally, metal grid electrodes are formed using a screen-printing method. By inserting the intrinsic a-Si layer, the defects on the c-Si surface can be passivated.

The HIT/HJT structure provides high performance with the National Renewable Energy Laboratory (NREL) reporting approximately 23% efficiency. In addition, HIT/HJT cells exhibit a better temperature coefficient compared to conventional p/n c-Si solar cells. This technology may become more interesting now that some of the original patents have expired.

Metal wrap through (MWT)[9]

MWT is one of many types of back contact technologies. In MWT cells, the front metal grids are wrapped through via holes to the rear side of the wafer, reducing shading and surface recombination losses. On MWT modules the strategy of full back side interconnection of the cells results in lower cell-to-module losses by avoiding much of the resistive losses in existing double-side interconnected H-pattern solar cells. The reported efficiency improvement using MWT is 0.3%.

Interdigitated back contact (IBC)[10]

IBC cells consist of a c-Si wafer and alternating lines (interdigitated stripes) of p-type and n-type doping. This cell architecture has the advantage that all of the electrical contacts to the p and n regions can be made on one side of the wafer. When the wafers are connected together into a module, the wiring is all done from one side. Efficiencies greater than 23% have been reported.

Another approach is to combine IBC with HIT/HJT (IBC-HJ). These cells have a very high efficiency potential of more than 24% on p-type and more than 25% on n-type wafers, respectively. The IBC-HJ cell structure consists of a contactless and well passivated front-side with a back-side of amorphous/crystalline silicon heterojunction contact structures.

One to watch

One of the ways to improve overall cell performance is to retain more of the photons that hit the cell surface. Easier said than done. A variety of techniques are used, often in combination, from forming random pyramids to AR coatings. A relatively new entrant is a process that involves the etching of nanopores into the silicon surface. This process results in a surface that captures a portion of the light that would normally be reflected off the usual AR coatings, including in low and diffuse light situations. Estimates are that close to 10% more photons can be harvested with fixed-angle installations. More photons reach the device, means more electrons are generated from the device.

Figure 2 shows the contrast between a commercial wafer with the standard pyramidal texture etch and the same type of wafer with a black silicon etch. The wafer on the left still requires a silicon nitride AR layer to be added in order to reduce the reflectance from about 10% to about 5%. The wafer on the right does not need an additional AR layer to be added and has an average reflectance of about 1% or less.

Figure 2: Pyramidal Texture Etch and the Same Type of Wafer with a Black Silicon Etch (courtesy of Natcore Technology)

Figure 3 shows a high magnification image of the cross section of a typical black silicon surface layer. Creating the layer is a wet process step. Figure 4 shows a similar cross section of a black silicon layer, but one in which the pores have been filled and overcoated with silicon dioxide. The silicon dioxide is a liquid phase deposition process (LPD) at moderate temperatures (< 60°C).

Figure 3: High Magnification Image of the Cross Section of a Typical Black Silicon Surface Layer (courtesy of Natcore Technology)

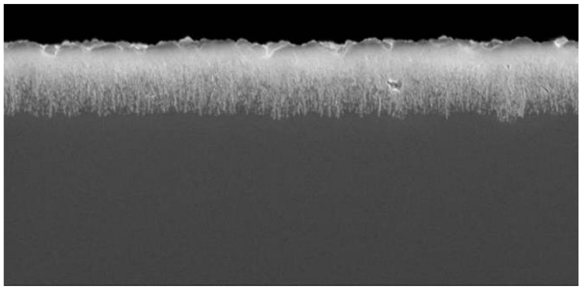


Figure 4: LPD Coated Black Silicon Surface (courtesy of Natcore Technology)

The silicon dioxide serves to passivate and protect the black silicon nanoporous structure. No further surface treatment is needed once the silicon dioxide has been deposited and the wafer is ready for the usual screen printed contact formation part of the cell line. The black silicon process is performed on a single wet station and eliminates the silicon nitride deposition step.

The step is obviously a cost, so the question is how can this process be integrated in a manner that makes it cost effective? Fortunately, in part, this is a replacement step; so, in order to be cost effective, it needs to be cost and value competitive relative to existing techniques. The combination of nanopore creation and deposition of a liquid phase oxide appears to be capable of being integrated into a single piece of equipment. The cost of the processes it may replace are thought to be approximately 10-12 cents per cell. Preliminary COO studies, including one later in this paper, have been performed for a black silicon process and the new process is competitive at 12 cents; with rounding errors, this translates to about $1 per conventional panel. If you can sell that panel for $1 more, then you have broken even. Even today, that is a relatively modest bar given the added light captured by the process.

References

1. I. Kashkoush, D. Jimenez, “Examining cost of ownership of crystalline-silicon solar-cell wet processing: texturization and cleaning,” Photovoltaics International, Ed. 7.
2. D. Jimenez, “Cost of Ownership and Overall Equipment Efficiency: A Photovoltaics Perspective,” Photovoltaics International, Ed. 6.
3. D. Brown, D. Jimenez, “Examining cost of ownership for front- and back-side metallization of crystalline-silicon solar cells,” Photovoltaics International, Ed. 8.
4. R. Kopecek, J. Libal, “Switch from p to n,” PV Magazine, Ed. 06/12.
5. W. Kessels, J. van Delft, G. Dingemans, M. Mandoc, “Review on the prospects for the use of Al2O3 for high-efficiency solar cells,” c-Si Workshop, Eindhoven University of Technology.
6. D. Appleyard, “PV Technology: Swapping Silver for Copper,” Renewable Energy World International, July 2012.
7. T. Falcon, “Getting More Charge from Solar: The challenges of selective emitter - Selective emitter approaches,” Solar Novus Today, December 7, 2010.
8. Y. Tsunomura, et al, “22%-Efficiency HIT solar cell,” PVSEC 17.
9. W. Zhao, et al, “Efficiency improvements by metal wrap through technology for n-type Si solar cells and modules,” 27th European Photovoltaic Solar Energy Conference, September 2012.
10. M. Scherff, “Novel methode for preparation of interdigitated back contacted a-Si:H/c-Si heterojunction solar cells,” 26th European Photovoltaic Solar Energy Conference, September 2011.

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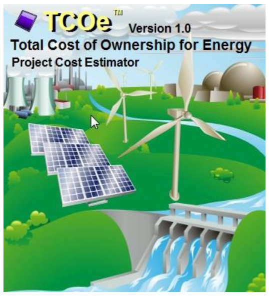
New WWK Article in Photovoltaics International

CIGS Manufacturing: Promises and Reality

Photovoltaics International's 21st edition will contain a paper written by WWK. This paper will be the sixth in a series covering business analysis for PV processes. The abstract is: Economic issues are the driving forces behind photovoltaic (PV) adoption. Even technological advances are measured against their impacts on cost per watt, levelized cost of energy (LCOE), and total cost of ownership for energy (TCOe™). In this paper, we look at two approaches to manufacturing thin film Copper-Indium-Gallium-diSelenide (CIGS) PV, sputtering and coevaporation, and their potential areas for cost improvement.

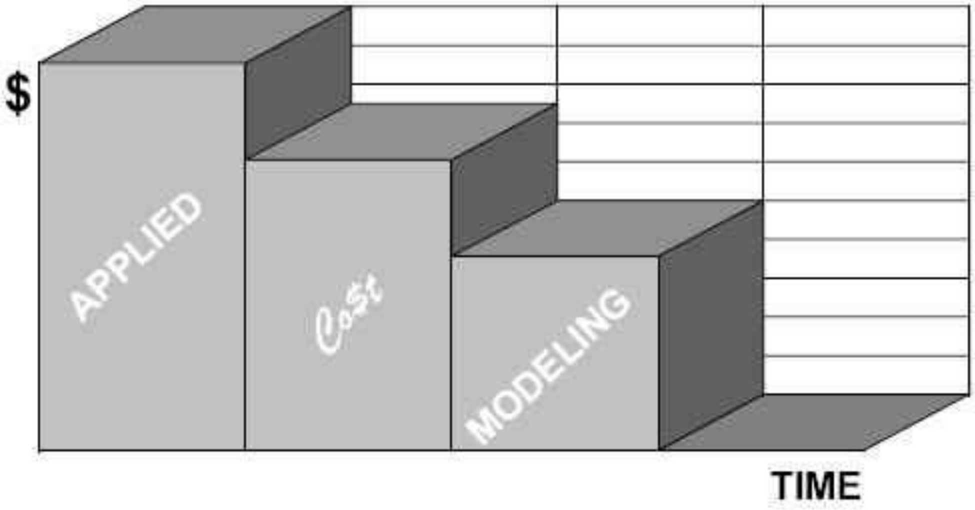
TCOe Used to Justify MLB Stadium Conversion to Solar

WWK just finished a study comparing grid power and PV for a major league baseball team's spring league facility in Arizona. With electric bills over $10,000/month, looking at solar was a logical move. The problem was that levelized cost of electricity (LCOE) showed a higher generating cost for PV than grid cost. Total cost of ownership for energy (TCOe™) also looks at the value of removing a cash use (i.e., payments to the local electricity company) as part of the lifetime return on investment (ROI). The more comprehensive approach of TCOe showed a positive net present value.



Breaking News: UNSW Added to WWK Customer Base

Just as ACM went to print, the University of New South Wales joined the ranks of WWK's worldwide Factory Commander customer base. UNSW will be using Factory Commander in the School of Photovoltaic and Renewable Energy Engineering in both teaching and research environments.



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