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Inside

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A Rapid Modeling Technique for Measurable Improvements in Factory Performance

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Abstract

This paper discusses a methodology for quickly investigating problem areas in semiconductor wafer fabrication factories by creating a model for the production area of interest only (as opposed to a model of the complete factory operation). All other factory operations are treated as “black boxes”. Specific assumptions are made to capture the effect of reentrant flow. This approach allows a rapid response to production questions when beginning a new simulation project. The methodology was applied to a cycle-time and capacity analysis of the photolithography operation for Siemens’ Dresden wafer fab. The results of this simulation study are presented.

Introduction

Discrete event simulation is an important tool for analyzing the characteristics of complex manufacturing systems. For semiconductor wafer fabrication facilities (fabs), simulation is becoming recognized as a way of impacting decision-making through factory performance analysis. Simulation is being used to determine how changes in production practices impact wafer throughput, tool utilization and cycle time. As in all simulation projects, collecting, preparing, maintaining, and analyzing data are keys to success.

The Siemens Microelectronics Center (SIMEC) in Dresden, Germany was in a production ramp-up phase and was experiencing large deviations from planned cycle times. In some cases, particularly

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in the photolithography and furnace operations, these deviations were not clearly understood. (See Figure 1) Production management decided to use simulation to investigate these problem areas. The photo area was chosen for deeper investigation because of it is the most capital intensive area in the fab and this time it was the bottleneck of the line. A Dresden project team from production, assisted by a technical simulation team from the Munich semiconductor headquarters, used Factory Explorer® to investigate cycle-time issues in the photo area. Factory Explorer is a simulation, capacity, and cost analysis application from Wright Williams & Kelly that has proven to be an effective tool for modeling semiconductor operations. The goals of the simulation project were to understand the deviation between planned and actual cycle time and to make recommendations for potential improvements in factory performance.

The simulation team suggested first creating a model of the entire fab operation, and then adding detail to the photo area as needed to answer specific questions. Believing that this approach would take too much time and the understanding of the detail would be not accurate enough, the production control management preferred to only simulate a small model and analyze cycle times within the separate process area. Behind this decision was also the request to clearly understand the single operation first, then the process area, and finally the whole factory. Management wanted a quick implementation to correct the current situation, and requested that attention be focused only on the immediate problem area.

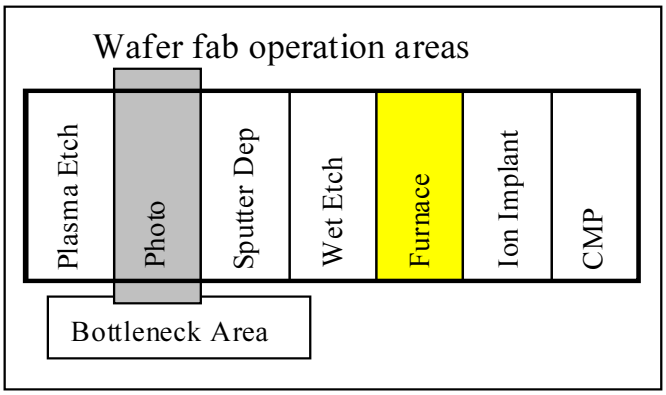


Figure 1: The problem area as a part of the fab

Therefore, it was decided to model only the photo process area. Additional justification for this decision came from the knowledge that the factory was in a production ramp. Since the situation was continuously changing, the input data for the model would need constant updating throughout the investigation. To insure that findings remained valid over time, the model needed to be kept current. The smaller, single-area, photo model would certainly require less effort to update than would a full factory model.

Model, Methodology, Assumptions

Modeling of semiconductor wafer fabrication, however, is somewhat complex because of the reentrant nature of the process flow (see Figure 2). In a typical fab, each wafer lot revisits the photo operation 15 to 25 times, with visits to other operations in between. The challenge for the simulation team was to create this photo-only model and somehow capture the effects of the reentrant flow.

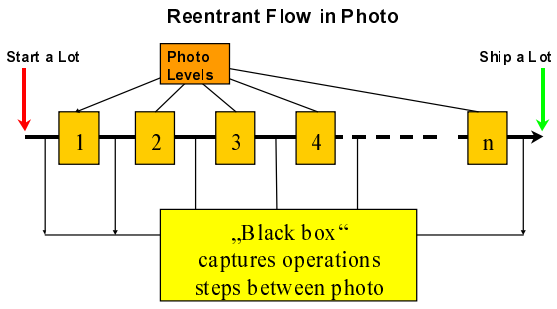


Figure 2: Reentrant flow in semiconductor manufacturing

To meet this challenge, a model was developed in which only the operations related to the photo area were fully described. Between each visit to photo, all other operations were assigned to one "dummy" step with a single piece of processing equipment. This "dummy tool" had an infinite number of servers. Part of a typical process flow is shown in Figure 3. Each dummy "operation" assigned a process time and a delay time based on averages of historical data retrieved from the Workstream™ manufacturing execution system.

N#	rework	operation	tool
1		Start a lot - to Photo level 1	dummy
2		Photo level 1	stepper cluster
3		CD line measurement	CD measure tool
	rework1	rework loop wet etch	wet etch bank
	rework2	rework inspection	microscope
4		Overlay measurement	OVLAY measure tool
	rework1	rework loop wet etch	wet etch bank
	rework2	rework inspection	microscope
5		Inspection Floodlight	microscope
6		Inspection Microscope	microscope
	rework1	rework loop wet etch	wet etch bank
	rework2	rework inspection	microscope
7		Photo level 1 to Photo level 2	dummy
8		Photo level 2	stepper cluster
9		CD line measurement	CD measure tool
	rework1	rework loop wet etch	wet etch bank
	rework2	rework inspection	microscope
10		Overlay measurement	OVLAY measure tool
	rework1	rework loop wet etch	wet etch bank
	rework2	rework inspection	microscope
11		Inspection Floodlight	microscope
12		Inspection Microscope	microscope
	rework1	rework loop wet etch	wet etch bank
	rework2	rework inspection	microscope
13		UV Harden	Hardener
14		Photo level 2 to Photo level 3	dummy
15		Photo level 3	stepper cluster

Figure 3: Organization of process flow

All process steps from lot release to the first entry into the photo area were combined into one dummy step in the simulation model. A mean process time for this dummy step was first determined by summing all raw process times of the actual production steps. A queue time, or delay time, was then calculated and added to this dummy step (as if it were part of the process time). The queue-time calculation multiplies the raw process time of each step by a lead time factor (multiplier-of-theoretical-cycle-time factor). The lead time factor was derived from historical data provided by the production group. The lead time factors used in the model correspond to the real flow factors achieved in the factory. The resulting queue time also includes travel times between operations. If adequate process time information for a particular process step was not available, estimates from the planning department were used.

The same procedure was used for the process steps between each subsequent photo operation. To account for variability in the reentrance into the different photo levels, different lead time factors were assigned for different product groups. Dummy step process times were drawn from a triangular distribution. To help decrease the model-building time, products with similar process routes were modeled as one product group, or family, at the appropriate combined wafer start rate.

Based on the factory's historical scrap rate, the average scrap rate for the step was assigned to each operation within the photo process area. Within each "black box" the number of scrapped wafers as a sum of the combined steps was assigned to the dummy step. Rework was modeled only for the photo steps and was based on the actual historical rework rate. No significant rework occurs outside of the photo area. Travel times within the photo area were not simulated because this area was not a concern of management and the additional detail would add no value to the analysis.

The model was validated against production department output reports from the Workstream™ system for recent reporting periods. Comparison between actual reports of photo equipment utilization from the fab and from the model showed an accuracy of 90%. Photo area cycle time comparisons showed the model to be 97% accurate when compared to actual fab data.

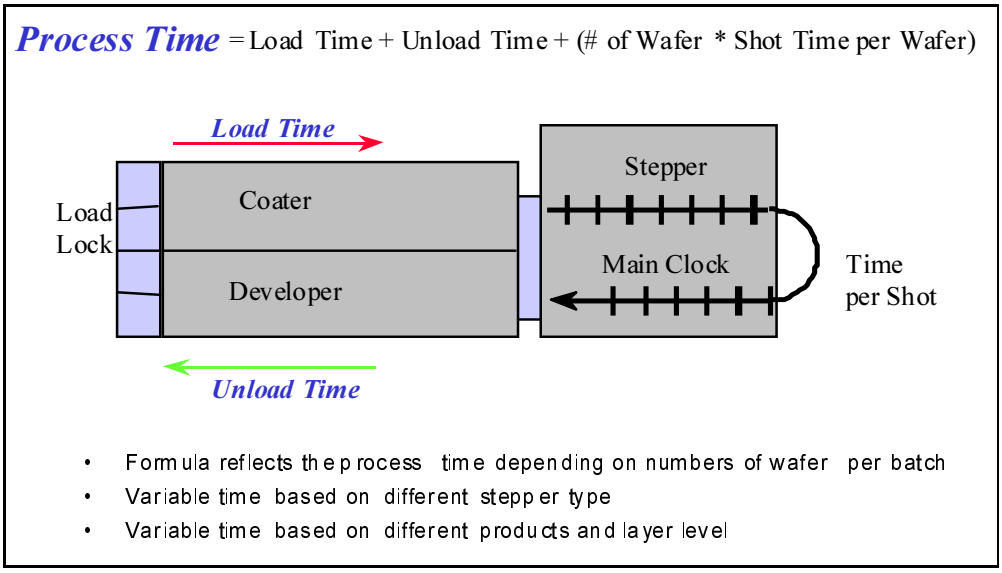
Next, a detailed study was done to understand the reasons for deviations between planned and actual cycle times and to make recommendations for improving factory performance.

Results of the study

Data Analysis

One of the direct benefits of applying discrete-event simulation in the factory is that data errors and opportunities for improving data collection are often uncovered. In this case, a detailed analysis of the input data for the simulation model resulted in a new formula for calculating cluster tool process times. (A cluster tool is illustrated in Figure 4.) The demand for a new way to calculate the times came from the manner in which the data was being used in the simulation model. The time study department was using lot-based times that did not account for several important influences and, therefore, were providing inaccurate calculations for equipment throughput and utilization. Photo cluster process times are now calculated based on type of product, batch size, number of shots per photo level, and exposure intensity. This gives a main clock time per wafer within the stepper and provides a much improved calculation for the industrial engineers.

Figure 4: Photo cluster tool process time calculation



The new formula has been proven to provide much more accurate output. It has subsequently been accepted for throughput calculation by the industrial engineering department and also by the stepper equipment manufacturer.

Stepper dedication

The photo manager was employing a stepper dedication policy based on both technological and logistical reasons. Some steppers, for example, were dedicated to the most advanced photo processes. Others were dedicated in an attempt to keep a balanced inventory flow to each machine. Simulation runs suggested that under current process times and product volumes a new dedication plan for the steppers would be beneficial. The model showed a 7.5 % increase in throughput due to this change.

The new dedication scheme has been introduced into the shop floor. Two stepper cluster tools are dedicated to test and evaluation lots and to new products (which usually need more engineering attention). For operations with long process times, additional tools are dedicated. The remaining steppers are available to run any product and process. Setup changes are made as inventory demands.

Dispatch analysis

The stepper cluster tool allows the operator to load as many as four lots per process run at an certain photolithography level. Existing operating policy (dispatch rules were priority lots first, then critical ratio, while following strict setup avoidance) caused the operator to normally run smaller batches than this. In practice, 70% of the time high-volume products were being loaded with only two lots per run. Only 10% of all runs had three or four lots per batch.

A "force full batch" rule was applied to the simulation model, which allowed the operator to take lots that were further down in the dispatch list in the interest of processing a full batch. This change slightly increased the variation of cycle times, but resulted in a higher throughput at the equipment. This allowed an increase in wafer start rates with no corresponding increase in average cycle times. An additional throughput increase was achieved by relaxing the setup avoidance policy so that a setup would be allowed if it resulted in a full batch. The model indicated a 10.5% increase in throughput from these changes in strategy. As shown in Figure 5, relaxing the setup avoidance policy is only beneficial when operating under the "force full batch" rule. Otherwise, the small batch sizes cause significant cycle time increases. Photo management has since implemented this recommendation.

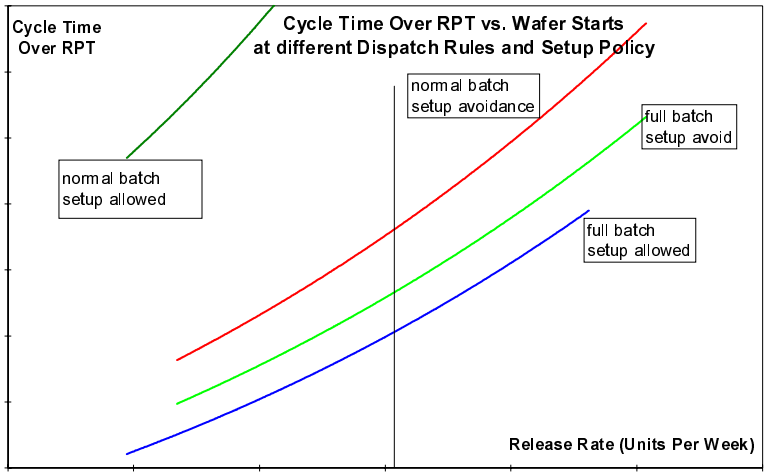


Figure 5: Impact of dispatch rules changes

What-If-Scenarios

The Dresden photo team has been working on rework reduction since fab start-up. The simulation model was used to help them measure the potential impact of success in this area and to set specific goals for reducing the rework percentage. After using existing rework percentages in the base model, several specific scenarios were run to determine the impact of achieving reduced rework rates. Figure 6 shows an example of potential improvements in throughput and cycle time. A reduction of 25% of the actual rework rate would lead to a 17% cycle time reduction, while eliminating all rework would reduce cycle time by up to 40%. Additionally, such improvements help reduce the cost per wafer.

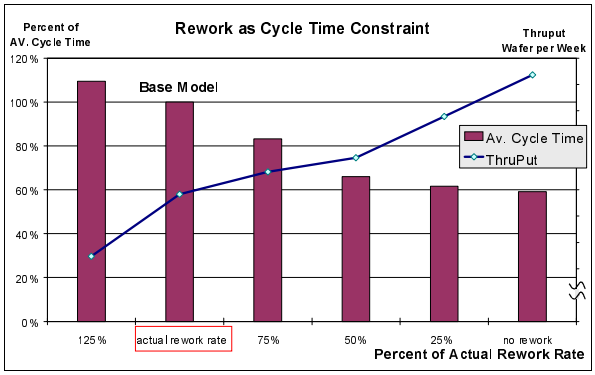
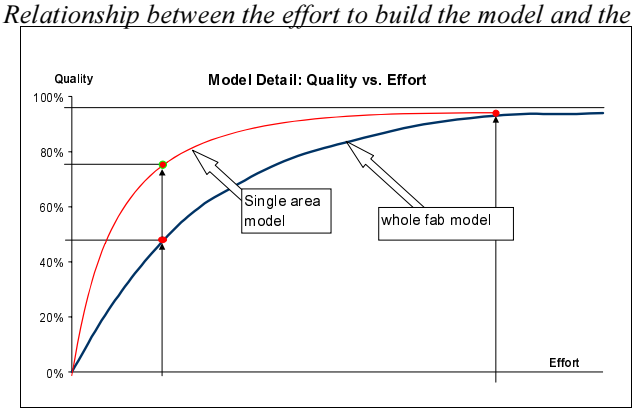


Figure 6: Impact of rework reductions on CT and Throughput

Conclusions

This study has shown the feasibility of simulating a single process area out of the whole fabrication complex and getting measurable recommendations for implementation. This methodology permits a more focused model to be built in the same time required to build a larger, less detailed model. The focused model is also easier to update, and allows a quicker reaction to specific factory problems (see Figure 7).

Figure 7: Relationship between the effort to build the model and the quality of results



A very important benefit of this project has been an increased understanding of the photo operations by all people involved: operators, process engineers, and managers. There is an increased knowledge of how the area functions and what mechanisms have the most influence. After pointing out the immense benefit of rework reduction, for example, the focus on reducing rework at critical photo levels is even stronger than before. Having more emphasis on details in the photo model allows fast investigation of problems in the line and easy updating of requested data. The simulation team believes that some findings would not have been detected if a full fab model had been constructed.

The Dresden fab has been able to increase available capacity by 15% with no increase in overall cycle time. Directly attributing this impact to the simulation team's recommendations is difficult because an aggressive production ramp and a variable product mix have created a constantly-changing factory over the relevant time period. In general, however, the authors feel that the implementation of this work has made a significant contribution to obtaining a higher throughput for the photo production area.

The success of this project has led to a factory-wide acceptance of the benefits of simulation. The Dresden site has since formed its own simulation team for continued analysis. The plan is for this team to add detailed models of each process area, ultimately leading to a model of the full fab. The team believes that a better understanding of each single process operation will lead to a much better understanding of the entire fab production process.

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MEMC Selects Factory Commander™ for Advanced Factory Cost Modeling

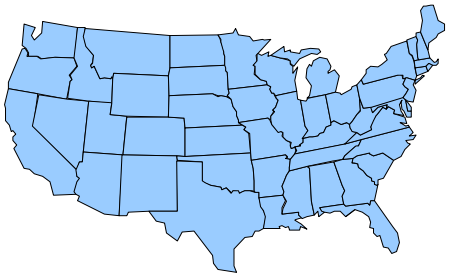
MEMC Electronic Materials, Inc., a leading supplier of silicon wafers used in the production of integrated circuits, announced today that it has purchased advanced factory cost optimization software from Wright Williams & Kelly. The software, Factory Commander™, will initially be used in the US and Japan to help optimize 300mm wafer process design.

According to Steve Brunkhorst, 300mm Product Manager at MEMC, “We will use Factory Commander™ to evaluate innovative 300mm technologies and select the most effective process. It will also enable us to accurately predict all costs associated with a particular process design prior to construction of a mass production facility. We know that the marketplace values MEMC’s robust approach to product design and cost engineering.”

“We are pleased to have MEMC join our rapidly growing list of Factory Commander™ customers,” stated David Jimenez, WWK’s President. “The massive investments associated with 300mm development are driving organizations to fully understand all the potential financial impacts. Factory Commander™ is helping companies like MEMC to manage this transition in a manner that will minimize the business risks. MEMC is the first silicon supplier to implement this strategy and I believe this reflects their focus on manufacturing excellence.”

MEMC is a leading producer of silicon wafers in the world. The silicon wafer is the fundamental building block of semiconductors, which, in turn, are found in virtually all electronics applications, including computers, telecommunications equipment, automobiles, consumer electronics products, industrial automation and control systems, and analytical and defense systems. Headquartered in St. Peters, MO, MEMC operates manufacturing facilities directly or through joint ventures in Italy, Japan, Malaysia, South Korea, Taiwan, and the United States.

U.S. Fab Location Can Make $200 Million Difference in Costs, Says Study



By J. Robert Lineback

This article was first published in Semiconductor Business News (SBN), Feb. 16, 1998 and is reprinted here with permission of SBN.

Local infrastructure and community support for a new $1 billion wafer fab in the United States can mean the difference of at least $200 million in operating costs over the lifetime of a semiconductor plant, according to a three-year study of U.S. chip-processing facilities.

The best chip companies in picking new wafer fab locations today are IBM Microelectronics, Intel, Motorola and Texas Instruments, while Asian chip makers—in particular South Korea's Hyundai Electronics Industries Co. Ltd.—have the worst track records in U.S. site selection, concluded the study. A summary of the study's findings appears in the February issue of Infrastructure , an industry financial and manufacturing newsletter that also has a Web site (http://www.infras.com).

The study of chip plants in Oregon, Texas, Virginia, Utah, California and other U.S. states concluded that local infrastructure and political support of chip manufacturing can make a big difference—especially if the wafer fab is producing high-volume commodity ICs, such as DRAMs.

"Hard" infrastructure, such as utilities and transportation systems, are relatively well understood by chip companies, but the study said most site selection efforts ignore "soft" infrastructure issues, which involves the local workforce, schools, hospitals and community services.

"Highly sophisticated semiconductor companies, who would not dream of buying a $1 million piece of equipment without detailed documented data about its cost-of-ownership, have often selected new fab sites usin g little more than the whims of top executives as primary criteria," said the summary of the report, which was authored by two former industry executives, who used pen names to conceal their identity.

One of the authors—identified as "Dr. Frederick Holstein"—is a former executive and founder of a large semiconductor capital equipment company in Silicon Valley. He spoke to Semiconductor Business News about the study, saying that Hyundai's fab in Eugene, Ore., has suffered from a number of mistakes, causing the plant to incur up to $300 million in excess costs.

But U.S. companies have also made mistakes too, according to the study, which partly blamed Digital Equipment Corp.'s decision to build its Alpha microprocessor plant in Hudson, Mass., as dragging down the RISC chip's success. The study said the plant is in a relatively high-cost location compared to other U.S. sites.

Among the key factors contributing to cost-of-ownership identified by the study was delays in completion of new plants and interruptions of operations. Currently, a 200-mm (8-inch) fab—capable of 25,000 wafer starts per month—costs about $1 million a day in expenses, said the study. By early next decade, those costs will escalate to several million dollars a day, meaning any delays or disruptions of operations due to weather or local infrastructure will be costly other the average lifetime of a fab, which is about 12 years, according to the study.

Cost of Test Simulation Software Released by WWK

Wright Williams & Kelly, the world's leading supplier of operational modeling software and consulting services, has announced that it is shipping its much anticipated PRO COOL® for Wafer Sort & Final Test. The software is designed to provide semiconductor manufacturers and test system suppliers the ability to determine the Cost of Test prior to purchase or design implementation.

PRO COOL® for Wafer Sort & Final Test is the next generation of Cost of Ownership (COO) software for test floor operations. PRO COOL® utilizes the world standard in COO software, TWO COOL®, to build descriptions of test cell components while integrating all test specific information into a single, unified software model. PRO COOL® answers these key questions:

What is the Cost of Test?

Which component of the test cell is the bottleneck?

What are the activities that drive test cell costs?

How many test cells are needed to meet demand?

What is the lot processing time?

PRO COOL®'s design allows the user to perform sophisticated capacity planning and analysis, including independent selection of start or ship rates, single test cell maximum capacity, or user specified number of test cells. Define a capacity ramp and PRO COOL® calculates the test cell installation plan.

Technical Presentations Focus on CMP Cost Drivers

David W. Jimenez, President of Wright Williams & Kelly, will be delivering a paper, ***CMP "Cost Drivers: An Overview of CMP Cost of Ownership"***, at CMP World '99 in San Jose, California, on Tuesday, November 2. He will discuss the following topics:

- Cost Impacts of Reliability, Equipment Costs and Markets
- Yield Issues and Cost Impacts
- Cost and Performance Trade-Offs
- Impacts of CMP

Wright Williams & Kelly will also be teaching a seminar, ***CMP Cost of Ownership***, at the CMP World '99 Conference in San Jose, California. The seminar will be conducted on Monday, November 1. You may register by contacting Intertech, 19 Northbrook Drive, Portland, ME 04105 USA - Phone 207.781.9800 or email info@intertechusa.com.

SEMI New and Revised Standards

SEMI announces the availability of the following new and revised standards that may be of interest to those involved in all areas of cost and operations modeling.

SEMI E10-0699E - Standard for Definition and Measurement of Equipment Reliability, Availability, and Maintainability (RAM) [Revised] This document establishes a common basis for communication between users and suppliers of semiconductor manufacturing equipment by providing standards for measuring RAM performance of that equipment in a manufacturing environment. The document defines six basic equipment states into which all equipment conditions and periods of time must fall. Equipment states are determined by functional issues, independent of who performs the function. The measurement of equipment reliability in this standard concentrates on the relationship of equipment interrupts to equipment usage, rather than the relationship of failures to total elapsed time.

SEMI E35-0299 - Cost of Ownership for Semiconductor Manufacturing Equipment Metrics [Revised] The purpose of this guide is to provide standard metrics for evaluating unit production cost effectiveness of factory equipment subsystems in the semiconductor industry. The guideline is appropriate for application to any type of equipment processing semiconductor units, which may be wafers, devices, or other material. The guideline establishes a well-defined practice to facilitate an understanding of equipment-related costs by providing definitions, classifications, algorithms, methods, and default values necessary to build a full or constrained cost of ownership (COO) calculator. The definitions provide a metric which can be applied to any factory equipment system, but are specialized to silicon integrated circuit wafer and device production. Effective use of the metric to build a COO model requires identification of the constraints, parameter values, and data values within the adopted category classification.

SEMI E79-0299 - Standard for Definition and Measurement of Equipment Productivity [New] The document provides metrics for measuring equipment productivity. The document defines the metrics and calculations for measurement of equipment productivity. In the context of this document, as with most discussions of equipment productivity, it is important to note that the term “equipment” refers to the entire context of a “node” of production capacity within the larger context of the fab. The tool or piece of equipment is only one component of that node. As such, it has become commonly used terminology to refer to the productivity of that node as “equipment productivity”, even though it is impacted greatly by factors far beyond the equipment itself. Effective application of this standard requires that equipment performance is tracked using the metrics for Equipment Reliability, Availability, and Maintainability (RAM) established in SEMI E10. This document is currently limited to measuring equipment productivity through Standard Overall Equipment Effectiveness [OEEs], but does not address the impact of productivity changes on cost, cycle time, or other measures.

A complete list of standards is available at www.semi.org