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Estimating the Costs, Benefits, and Return on Investment of Integrated Semiconductor Process Metrology

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Executive Summary

Cost of ownership (COO) was developed to address the economic and productive performance of a fabrication tool by estimating the total life-cycle cost of a specific semiconductor process step. But COO for equipment required to support manufacturing such as metrology tools is also needed. With a few modifications, COO can be applied to integrated metrology systems as well[1]. COO analysis for integrated metrology is more complex than for fabrication equipment, requiring a two part analysis. First, the costs of operating the tool with and without metrology are estimated. Second, the cost impact of metrology on the processes being measured must be estimated. The benefits of integrated metrology are estimated by considering the impact of metrology on a process or product. When characterization information improves the process, metrology adds value to the process.

Overview of Cost of Ownership

SEMI E35 defines COO as the full cost of embedding, operating, and decommissioning, in a factory and laboratory environment, a system needed to accommodate a required volume[2].

Editorial Board

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1999 Calendar of Events

April

13-15 SEMICON Europa
Munich, Germany

14 SEMI-sponsored seminar
"Understanding and Using Cost of Ownership"
Munich, Germany

15-16 SEMI-sponsored seminar
"How to Successfully Manage New Product Introductions"
Munich, Germany

May

4-6 SEMICON Singapore

July

9-10 SEMI-sponsored seminar
"How to Successfully Manage New Product Introductions"
San Francisco, California

12-14 SEMICON West - Wafer Fab
San Francisco, California

12 SEMI-sponsored seminar
"Understanding and Using Cost of Ownership" for Wafer Fab
San Francisco, California

14-16 SEMICON West - Assembly & Packaging
San Jose, California

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San Jose, California

October

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"Understanding and Using Cost of Ownership"
Austin, Texas

November

8-10 SEMI-sponsored seminar
"Managing and Marketing After Sales Support"
Mt. View, California

The significant COO inputs include:

- Equipment cost
- Operating cost
- Yield
- Down time
- Throughput rate
- Value of completed unit
- Cost of discarding a good unit
- Cost of shipping a bad unit

These factors are combined in the COO equation[3]:

$$COO = \frac{CF + CR + CY}{L \times TPT \times Y \times U} \quad (1)$$

where:

COO = Cost per good unit

CF = Fixed Cost

CR = Recurring Cost

CY = Cost of Yield Loss

L = Equipment Life

TPT = Throughput Rate

Y = Yield

U = Utilization

Fixed costs are incurred once during the life of the system and are associated with the acquisition and installation of equipment. Fixed costs include costs such as equipment purchase, installation and setup, facility modifications, initial training, and initial calibration costs. Recurring costs are incurred on an accrued basis. Recurring costs such as material, labor, repair, standards, calibration, utility and overhead expenses are costs that are incurred during equipment operation. Cost of yield loss is the value of scrap caused by the process step. Process scrap identified at the step of interest but caused by prior processing is part of the prior process tool COO. Thus, yield losses caused by the processing tool must be clearly separated from prior losses. The sum of these costs form the numerator of the COO equation.

The denominator of equation (1) is an estimate of the number of good units produced during the life of the system. Throughput rate is based on measurement and handling times such as sample preparation, loading and unloading, reporting, and other overhead operation. It excludes training, repair, and calibration times since these are included in utilization. Yield may be defined as the ratio of good units compared to the total number of units produced, including rework. Utilization is the ratio of actual usage compared to total available time. Utilization includes repair and maintenance time, both scheduled and unscheduled; setup and calibration time; and standby time. It shows the impact of non-productive time on cost and normalizes ideal throughput to a realistic estimate. Utilization is estimated using SEMI E10 definitions for availability, reliability and maintainability[4].

For metrology, COO may be described in terms of cost per measurement. For a 100% sample, cost per device equals cost per measurement, but for less than 100% samples, the cost per device is some fraction of the cost per measurement.

Impacts of Metrology on the Process

Since the process and metrology are in series, process throughput depends on metrology methods. Further, since the process requires measurement, there is an impact of measurement on WIP. *See Table I.* WIP inventory between a process step and subsequent inspection is at risk if the process drifts. Several operating methods minimize that risk. Send

Table I
Sample Plan Impact on Process [5]

Sample Plan	Throughput	Utilization	α/β Risk
100%	High	Low	Low
1 of N	Low	Low	High
N per day	Low	Low	High
N per event	Low	Low	High
Send ahead	High	High	Low
In-situ	Low	Low	Low

ahead (or look ahead) samples* eliminate WIP risk but reduce process throughput and utilization. Integrated in-situ metrology operation minimizes risk with very little impact on utilization.

Since product or process yield at subsequent steps depends on the accuracy of metrology, we must consider the costs of discarding a good device and the cost of accepting a bad device. Measurement risk is illustrated in Table II[6]. Minimizing the cost of shipping a bad device is one purpose of metrology. However, if the sampling plan or methods are insufficient, bad devices will be shipped. But if specifications are too restrictive, then good devices may be rejected. Guard banding specifications increases α probability in order to decrease β probability.

The cost of discarding a good device is estimated by:

(2)

$$C_{\alpha} \quad \alpha \times WIP \times 9_{p}$$

where:

Cα = Cost of discarding good device

α = Probability of discarding good device

V_p = Value of device at metrology

WIP = Work in process

and the cost of shipping a bad device may be estimated by:

Table II
Measurement Risk

True State	Measured Result	Error
Good	Good	None
Bad	Bad	None
Good	Bad	Type I (α)
Bad	Good	Type II (β)

(3)

$$C_{\beta} \quad \beta \times WIP \times 9_{c}$$

where:

$C_β$ = Cost of shipping bad device

β = Probability of shipping bad device

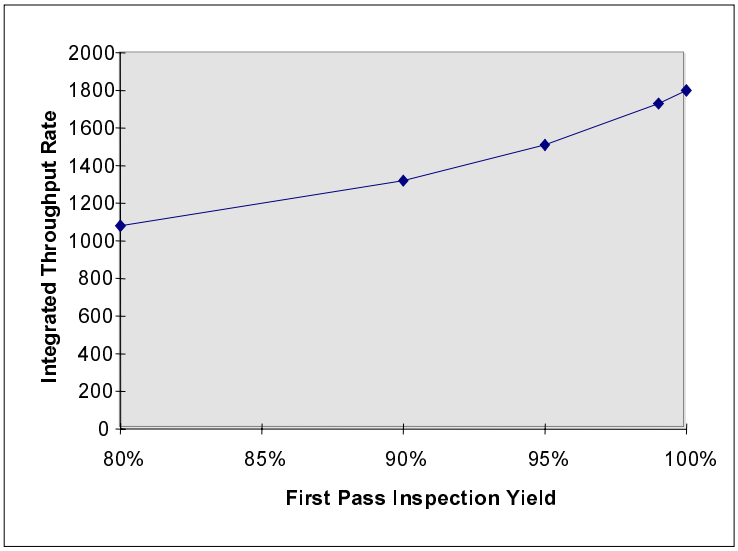
V_c = Value of replacement device

WIP = Work in process

The probabilities of discarding a good device and of shipping a bad device are related to the variance of the measurement. These probabilities may be reduced by reducing variance, increasing sample size, or developing more robust processes.

Impacts of Integration

Comparing integrated inspection strategies with nonintegrated methods allows the user to determine the costs and benefits of manufacturing integration. One impact of



Assembly Throughput Rate vs. Inspection Yield

* A send-ahead sample requires one or more wafers be processed, then submitted for measurement. The remaining wafers in the lot wait until the results of the measurement are complete and the equipment is adjusted. Only then will the remaining wafers in the lot be processed.

integration is the impact on throughput rate. Throughput rate is another important COO driver. Lower inspection yields will have a greater impact on throughput rate than higher yields as shown in the following example based on device assembly analysis[7].

Return on Investment Analysis

The two part COO for metrology analysis allows comparing the benefits of metrology with the metrology COO to estimate the return on investment (ROI) in metrology. Most of the costs of metrology are captured by the basic COO equation. These costs are expressed in terms of cost per measurement. The benefits of metrology are estimated by considering the impact of metrology on a process or product. The knowledge gained by characterizing a process or product lead to the following benefits:

- Reduced cost of shipping bad device
- Reduced cost of rejecting good device
- Improved sample methods
- Improved process throughput
- Reduced impact of mis-measurement on WIP

Return on metrology investment may be described by the following simple equations:

$$ROI = \frac{B_{Product} + B_{Process}}{MetrologyCOO} \quad (4)$$

Knowledge gained through metrology adds value to the process or product through continuous learning and improvement. Thus if characterization information improves the process, then metrology is a value added step.

In-Situ Particle Measurement Example[8]

The prevention and reduction of contamination are critical steps to the improvement of manufacturing productivity. Contamination-related scrap losses result in lost equipment productivity and increased wafer cost. Contamination increases COO by:

- Increasing maintenance and downtime
- Increasing equipment costs
- Increasing scrap loss

Standard measurement and control methods to monitor in-process particle contamination include particle count monitors and test wafers. These impact the productivity of manufacturing equipment. Running particle monitoring wafers may use about 5% of daily production time, more than 8 hours per week of lost production. Table III illustrates

Table III
Particle Monitoring Impact on COO

	External Measurement	In Situ Measurement
Tool and Metrology Equipment Cost	$1,000,000	$1,000,000
Tool Throughput	15 wafers/hour	15 wafers/hour
Productivity Impact	5%	0%
OEE**	86.8%	91.0%
COO	$4.57	$4.38
Depreciation	$1.27	$1.21
Maintenance	$1.02	$0.98
Floor Space Costs	$0.84	$0.80
Labor	$0.82	$0.79

** Overall Equipment Effectiveness

Table IV. Conservative COO estimate for a bottleneck epitaxial silicon CVD tool comparing current production methods, with production augmented by integrated epitaxial thickness metrology.

	Standalone	Integrated	Savings
COO (cost per good epi wafer)	$18.58	$17.42	$1.16
Product wafers per month per tool	15,257	15,823	566
Cost of Sales per Month	$1,351,486	$1,383,219	$31,733
Gross Revenue per month	$1,525,672	$1,582,254	$56,581
Gross Profit per month per cluster tool	$174,186	$199,035	$24,849
Installation Cost for integrated metrology	$0	$100,000	
Payback time for integrated metrology technology installation (months) Capital cost relative to gross profit method	4.0		
Wafer Selling Price	**100**	100	
Epi price premium over epi substrate	**30**	30	
Average Monitor wafer price (mostly reclaims)	**40**	40	
Tool Throughput (W/H)	**27**	27	
Tool Life (Y)	**5**	5	
Fixed Cost	$5,200,000	$5,300,000	$100,000
Cost of Yield Loss (Scrap)	$4,817,912	$4,734,303	-$83,610
Monitor wafer costs	$1,132,458	$774,981	-$357,476
Recurring Costs (excluding monitor wafer costs)	$5,010,000	$4,943,600	-$66,400
Scrapped wafers	45,770	45,094	-676
Utilization - OEE	77.41%	80.28%	
Yield	**95.00%**	**95.25%**	
Test Wafer percentage	**3.00%**	**2.00%**	
Downtime Sheduled	**2.00%**	**2.00%**	
Downtime Unscheduled	**4.00%**	**3.00%**	
Waiting for metrology	**4.00%**	**3.00%**	
Setup	**2.00%**	**2.00%**	
Idle	**4%**	**4%**	

the difference between in-situ and external particle monitoring methods in terms of cost per wafer.

In this example we estimated the impact of metrology by comparing the COO of the process step with external metrology and with in situ metrology. We assumed that the total cost of the process tool and the metrology systems were that same in both cases. We also assumed that yield loss and maintenance downtime were the same. These very conservative assumptions still results in a COO that is 4% lower with in situ metrology[***].

Cost of Ownership Model for Epitaxial Silicon Fabrication with Integrated Wafer State Metrology

This section describes a calculation of the cost and benefits of integrated film thickness monitoring for the epitaxial silicon process. The calculation details the potential impact of installing the On-Line Technologies ***Epi On-Line™*** integrated FTIR film thickness monitoring system on the Applied Materials Epi Centura HT 200 mm single wafer epitaxial silicon CVD cluster tool. We calculate both the cost impact of installing the film thickness monitor on the cluster tool and the impact to the cost of the process itself in terms of yield costs, test wafer consumption, increased utilization, etc.

The analysis showed that one key factor in evaluating the benefit of the tool involves whether the tool in question is a bottleneck tool. If the tool is a bottleneck to the overall

[***] TWO COOL® data files for all examples in this paper are available upon request from WWK. Request "Integrated Measurement Examples" by email to support@wwk.com.

manufacturing process, i.e. if demand exceeds capacity for the process, then even modest increases in tool utilization translate into significant gains in cost of ownership and profitability. Further gains are provided by reduced recurring costs involving monitor wafers, yield losses and consumables. If the tool is not a bottleneck, i.e. the tool sits idle waiting for incoming product and work orders much of the time, then increases in wafer per hour throughput result in increased idle time, and the benefits of increased production capacity are not fully realized. The savings in this case come primarily from reduced consumables, labor, and yield costs.

The assumptions and results in the cost of ownership model are summarized in Table IV for the case of a bottleneck tool. We have (conservatively) assumed that the integrated metrology will be installed as an augmentation to existing metrology and that no savings are to be had by eliminating the capital costs of the metrology processes already in place within a factory. The savings are gained through reduction of test wafers used to tune up thickness, reductions in routine monitor wafers, higher equipment utilization through reduced waiting times for metrology and a higher proportion of product wafers to test wafers. 100% real-time monitoring of epitaxial thickness will improve yield by identifying and classifying out-of range process chambers more quickly, before more wafers are misprocessed and scrapped. The particular numbers presented represent typical values for the commodity p/p+ epitaxial silicon industry, and were obtained from discussions with several silicon suppliers. Estimates of reduced monitor wafer usage, reduced labor, yield loss and other benefits were obtained through analysis of the beta site operations at Wacker.

Table V shows a similar calculation for which the tool is assumed to operate at chronic under-capacity. In

Table V. Conservative COO estimate for a non-bottleneck epitaxial silicon CVD tool comparing current production methods, with production augmented by integrated epitaxial thickness metrology.

	Standalone	Integrated	Savings
COO (cost per good epi wafer)	$15.01	$14.32	$0.69
Product wafers per month per tool	**15000**	15000	0
Cost of Sales per Month	$1,275,167	$1,264,753	-$10,413
Gross Revenue per month	$1,500,000	$1,500,000	$0
Gross Profit per month per cluster tool	$224,833	$235,247	$10,413
Installation Cost for integrated metrology	$0	$100,000	
Payback time for integrated metrology technology installation (months) Capital cost relative to gross profit method	9.6		
Wafer Selling Price	**100**	100	
Epi price premium over epi substrate	**30**	30	
Average Monitor wafer price (mostly reclaims)	**40**	40	
Tool Throughput (W/H)	**30**	30	
Tool Life (Y)	**5**	5	
Fixed Cost	$5,200,000	$5,300,000	$100,000
Cost of Yield Loss (Scrap)	$1,800,000	$1,710,000	-$90,000
Monitor wafer costs	$1,500,000	$1,017,995	-$482,005
Recurring Costs (excluding monitor wafer costs)	$5,010,000	$4,857,200	-$152,800
Scrapped wafers	45,000	42,750	-2,250
Utilization - OEE	68.49%	68.49%	
Yield	**95.00%**	**95.25%**	
Test Wafer Percentage	**4.00%**	**2.75%**	
Downtime Sheduled	**2.00%**	**2.00%**	
Downtime Unscheduled	**4.00%**	**3.00%**	
Waiting for metrology	**4.00%**	**3.00%**	
Setup	**2.00%**	**2.00%**	
Idle	**13%**	**16%**	

this mode of operation, the orders received, or some other external factor determines the level of production, and small changes in tool throughput translate into small variations in tool idle times. Improvements in tool productivity that translate into financial benefit then are those that impact consumables such as monitor wafers and chemicals, or recurring costs such as labor.

Discussion

The calculations shown in Tables IV and V show that substantial potential savings are to be had via the introduction of integrated film thickness metrology, but the magnitude of the savings depends greatly on the details of the operation. Though the SEMATECH specification for cost of ownership does not address the issue of bottlenecking, the most significant potential gains in productivity hinges on whether or not the tool is operated in bottleneck mode. In a well planned facility, any given tool is likely to bottleneck production at some time or another, but the exact percentage of time in which this situation occurs depends on many factors that are difficult to control (including an unpredictably fluctuating demand for wafers). In circumstances when capacity exceeds demand, there may be substantial benefits to shutting down a tool for extended periods, this may put the remaining tools in a near bottleneck state, depending on the instantaneous demand and the cost to recommission a tool that has been shut down for extended periods. Labor reduction and test wafer elimination were also found to be significant drivers for integrated metrology. Monitor wafer usage and labor practices tend to be very fab dependent, and to properly estimate these parameters, close interaction with the fab management is required.

Payback times were calculated in terms of profit generated by the process vs. the additional fixed cost to install the integrated measurement system. For a tool operating as the production bottleneck, the estimated payback time to install the integrated measurement system was 4.0 months. For a tool operating at significant under capacity, the payback time expanded to 9.6 months.

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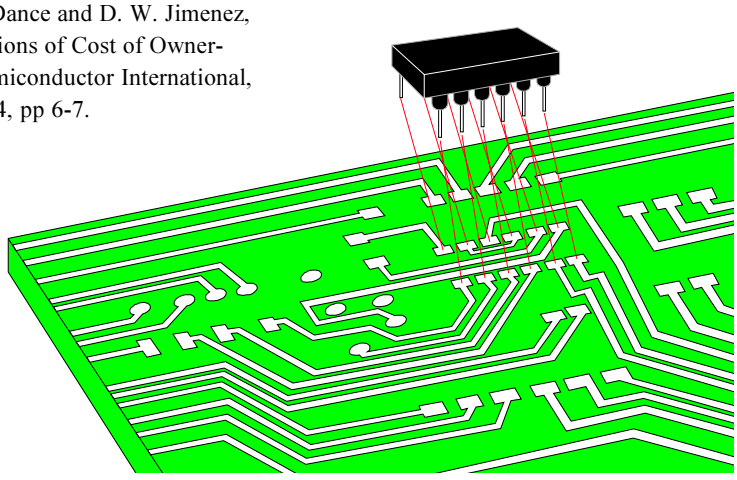

Reliability, Availability, Maintainability: Semiconductor Manufacturing Equipment Can Improve . . .

by Daniel M. Deans

When he was chief operating officer of SEMATECH, Jim Owens showed a set of curves illustrating the critical need to improve equipment productivity to enable the semiconductor industry to stay on the Moore's Law curve. Equipment Reliability, Availability and Maintainability (RAM) is a key component of productivity that is within the influence of the equipment manufacturer. Only recently, however, has the need for overall equipment effectiveness (OEE) driven the semiconductor manufacturing equipment industry to reconsider the importance of RAM engineering. Semiconductor manufacturing equipment has always been driven primarily by process technology and time-to-market requirements, with RAM performance viewed as a lower priority. As long as manufacturing tools met customer process performance specifications, unscheduled downing events every 100 to 250 hours were managed by relying on equipment supplier maintenance support to minimize downtime.

In a typical fab of 400 to 600 tools, all of which might have a similar mean time between failure (MTBF), this practice was considered barely tolerable if production output targets were met. However, today's cost pressures necessitate a new strategy. Fab management is now demanding better RAM performance from manufacturing tools, and tool suppliers are beginning to emphasize product RAM performance. These changes, along with the transition to 300 mm wafers, place considerable pressure on revenues and profits. Reliability engineering has long played a major role in systems development within the aerospace and automotive industries. Fortunately, application of RAM methodologies and established RAM engineering tools can prevent these pressures from adversely impacting the bottom line.

The MTBF Myth

Reliability engineering has always included systems analysis and modeling, and the fab can be analyzed as a system. Modeling the fab manufacturing processes to depict the relationships among tools (depending on tool numbers, how they are utilized and whether they are choke points) reveals the difficulty of meeting production targets in the typical scenario. Some companies believe that a point of diminishing returns is reached when the MTBF of a single process tool reaches 250 hours. Assuming that each tool provides an MTBF of 250 hours, and that there are 600 tools in the fab, the overall "fab MTBF" is less than 10 hours. Somewhere in the fab, a line is affected approximately every 10 hours by a downing event. Fab management has realized that this rate must improve, and tool manufacturers are being asked to help make it happen.

Engineering Economics

Each hour of unscheduled downtime increases costs and reduces profits. If a manufacturing tool that runs 250 hours without an unscheduled downing event were to operate 24 hours a day, seven days a week, the tool would fail approximately every 1.5 weeks. If the tool can be restarted within eight hours (conservative, according to some statistics), it would incur approximately 24 hours of unscheduled down time each month, or 288 hours a year. This, coupled with engineering time, scheduled down time, and other unproductive times, leaves the typical tool out of production far more than expected. Unscheduled down events incur, on the average, at least five times the overall cost of scheduled downs. Extending the above scenario to include all tools in a fab reveals a significant cost driver. If we can lower the unscheduled component of down time, the fab's bottom line will improve greatly, as will the total cost of ownership (COO) of the tool.

Semiconductor equipment suppliers must improve current designs to address dominant hardware and software failure modes while meeting demands for new products. The problem in many cases is the lack of an integrated design approach that includes reliability engineering disciplines to ensure that RAM requirements are addressed throughout the product development cycle. Solving this problem leads to reduced warranty and

other service-related costs for the equipment manufacturer and provides the industry with a product that exceeds requirements, increases productivity, decreases cost of ownership and boosts customer satisfaction.

There is a Solution to The Problem

Implementation of RAM processes and engineering techniques have been proven repeatedly in other industries and are easily applied to semiconductor manufacturing equipment. Doing so requires a reasonable level of buy-in and commitment within a company, education concerning RAM disciplines, and effective communication among all involved. Incorporating RAM expertise from company resources or as an outsourced function is essential; this expertise serves to help implement a RAM process such as that shown in Figure 1. This process, based on the Reliability Analysis Center Blueprints (Rome Air Development Center), has been developed and proven by the U.S. Air Force and NASA, and successfully applied in other industries to produce dramatic improvements in RAM

The 12-Step Process

Successful, systematic RAM application starts at the beginning of the product development cycle. Fortunately, products can be shipped to the field with excellent RAM performance without a major shift in the development schedule, meeting time-to-market requirements. Fielded products can also be improved using existing RAM methodologies. More about this in Step 12.

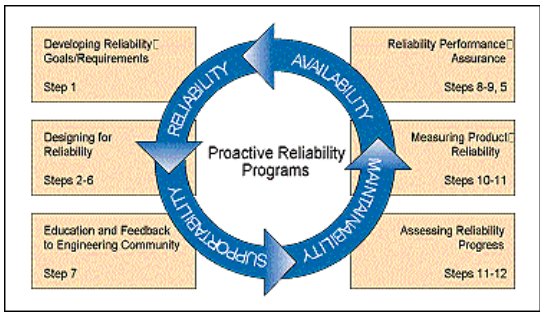

Figure 1. Overall Process for RAM Success

The following 12 steps have proven to be integral parts of a high reliability product development and release (PDR) cycle.

Developing Reliability Goals/Requirements:

1. Requirements Development and Allocation - The PDR process must include thoroughly understanding customer requirements. MTBF, availability (uptime) and mean time to repair (MTTR) requirements are equally important to etch rates, selectivity, strip rates, etc. RAM specialists must work with the marketing team to understand customer RAM requirements, provide and allocate these requirements to the lowest level of the proposed design, and provide design engineers with a roadmap to meet RAM allocations or "targets". Many critical design decisions will be made based on these allocations. This is similar to an error budget or tolerance stackup analysis, and is part of one of the key requirements of ISO 9001 for control of design inputs.

Designing for Reliability:

2. Design Input - RAM specialists must work with design engineers to ensure that requirements are met. This includes the use of proven RAM design practices, identifying and eliminating failure modes, selecting proper components, integrating interfaces and facilitating communication between hardware and software designers.

3. Design Standards and Proven Practices - The use of known and documented standard design practices incorporating lessons learned from fielded products is essential to RAM improvement. Knowing what provides optimal RAM performance, documenting it and ensuring that the design staff has access to the information are essential parts of an effective design document control system.

4. Design Assessment Through Trade Studies - This ensures that all design possibilities and the RAM characteristics of each are explored. Sometimes, the best design is the "less elegant" design scenario that was not considered.

5. Analysis as a Design Component - RAM analysis must be conducted throughout the design process. RAM specialists perform predictions; trade studies; failure modes, effects and criticality analysis (FMECA); tolerance stackup and other analyses that benefit the design and provide valuable information for use throughout the product's lifetime.

6. Preferred or Qualified Suppliers and Parts Lists - This ensures proper component selections and confidence in procured items. Establish a list of vendors who continually provide superior products from a RAM standpoint and generate preferred parts lists from those suppliers.

Education and Feedback to the Engineering Community:

7. Education Programs - RAM specialists should be constantly spreading their knowledge, especially to the design engineering staff. Personnel involved in the PDR process should be aware of the best in tools and techniques and should have access to customer feedback on successes and issues with previous designs.

Reliability Performance Assurance:

8. Supplier Control/Reliability Program Assessment - Take an active role in suppliers' RAM activities; share the goal of meeting customer requirements. Suppliers can provide the required level of performance when open communication exists and requirements are understood.

9. Failure Reporting And Corrective Action System (FRACAS) - A database and process that allows for corrective action based on disciplined root cause analysis of failures. This system must be closed-loop, meaning that problems are worked to completion and all appropriate personnel are involved in problem closure.

Measuring Product Reliability:

10. Test and Checkout Programs (Including Burn-In) - A critical step that is sometimes overlooked. New designs must be tested at several levels, and manufacturing tests such as burn-in and product checkout must be performed to eliminate infant mortality issues before the product is shipped to the customer.

11. Field Data Collection and Feedback - Provides important data for future designs, reliability growth, and sales/marketing efforts. Collection of field RAM data and feedback of that data to the engineering function in the company can help improve products and maintain a competitive edge.

Assessing Reliability Progress:

12. Upgrades Program - Also known as reliability growth, this step applies to fielded products. Companies should constantly look for ways to improve existing products. Hardware and software RAM performance improvement can significantly affect production cost metrics.

The Bottom Line

Costs include acquiring the proper RAM expertise, staff education and training, and establishing management support of data collection, analysis, dissemination and feedback systems. Return on investment can be large, and the time to implement the required processes and realize significant benefits is short. Recognition by customers for these activities will be positive, since improvement of tool performance in their fabs directly affects their bottom line.

Development and implementation of a well founded, complete RAM program is only as difficult or expensive as a company chooses to make it. If management embraces it with vigor and sincerity, success is the only predictable outcome. However, as with any new way of doing business, there are some costs associated with the learning curve. These costs will be paid, either through internal development of tools and techniques, or through the use of skilled, experienced outside resources to show the team how it is done; train the team in existing, proven tools and techniques; and coach the team in their effective, timely implementation.

About the Author ...

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Also contributing to this article was James A. Irwin, Irwin Consulting.

Wright Williams & Kelly Offers Solutions to Tyecin Systems' Clients

Wright Williams & Kelly (WWK) announced it is immediately offering significant discounts and incentives on its Factory Explorer® simulation software products and services to existing ManSim™ and TestSim™ customers. This action was taken in response to the recent layoffs and facility closures announced by Manugistics (NASDAQ: MANU), the parent of ManSim™'s developer, Tyecin Systems.

"We believe the closures and layoffs will have a negative impact on past and current ManSim™ and TestSim™ users," states David W. Jimenez, WWK's Vice President & General Manager. "Our current offer allows these users to switch to our Factory Explorer® product at minimal cost while continuing to do business with a company headquartered near Silicon Valley."

Factory Explorer® is an integrated factory analysis tool designed to help make smart business decisions. It is capable of directly reading ManSim™ user data files. The Factory Explorer® capacity analysis engine quickly predicts system capacity and bottleneck resources; the cost analysis engine calculates product cost and factory gross margin; and the fast discrete event simulation engine estimates dynamic measures such as cycle time, work-in-process, and waiting times.

Wright Williams & Kelly and SEMI® Offer Training Classes at SEMICON Europa

Wright Williams & Kelly and SEMI® have once again teamed to offer industry leading seminars at SEMICON Europa. The seminars offered by WWK will include "How to Successfully Manage New Product Introductions" and "Understanding and Using Cost of Ownership."

"How to Successfully Manage New Product Introductions" was developed in response to the clear difficulties and risks associated with the introduction of next generation products. The course provides mid- and senior-level managers involved in product development and introduction with a framework within which to maximize their opportunity for success. Class information and sign-up can be accessed at http://www.wwk.com/events.html

"Understanding and Using Cost of Ownership" provides a solid framework on COO from concepts through applications to hands on exercises. This course has been adopted as the exclusive COO training program for Texas Instruments, Philips Semiconductor, and STMicroelectronics, as well as numerous other industry leaders. Class information and sign-up can be accessed at http://www.wwk.com/events.html

Wright Williams & Kelly Adds Another Top 10 IC Manufacturer to its TWO COOL® Customer List

Wright Williams & Kelly (WWK) announced it has shipped a multi-site license for TWO COOL® to one of the world's largest semiconductor manufacturers. The client will use TWO COOL® to establish consistent and effective equipment cost criteria for future purchases and upgrades. Further details will be released pending final approval of content by the client.

PRO COOL® v1.1.2 for Process Sequences Ships

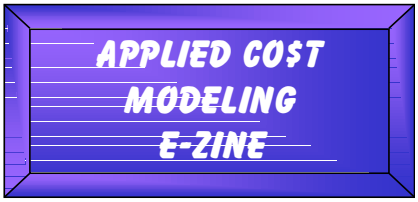
Wright Williams & Kelly (WWK) announced it has begun shipment of the latest version of its process flow cost modeling software. PRO COOL® v1.1.2 is provided free of charge for customers covered by warranty and maintenance agreements. Updates to the software include fixes to mode calculations, batch times on the minimum cycle time report and chart, and capacity calculations to allow more accurate estimates of low yield process flows.

PRO COOL® v1.1.2 for Wafer Sort and Final Test Readies for Shipment

Wright Williams & Kelly (WWK) has entered the final phase of certification for its new software for calculating the cost of test. PRO COOL® v1.1.2 for Wafer Sort and Final Test is the industry's first new test floor COO program since 1993. The software utilizes a completely new design allowing users to configure test cells on the fly without impacting basic COO data inputs. Automatic sensitivity analysis is also included for major performance factors. Customers with current maintenance agreements for COOL® ONE for Wafer Sort and Final Test will receive this upgrade at no additional charge.

Applied Co$t Modeling Now an E-Zine

Starting with the March 1999 issue of *Applied Co$t Modeling*, primary distribution will be available via internet download http://www.wwk.com/acm.html. Paid subscribers will continue to receive hardcopy versions of *Applied Co$t Modeling*. WWK is offering the download on a "shareware" style basis. If you like what you see and want to continue to download future versions, we ask that you consider payment per the schedule on page two of the publication.



News!

MAJOR 300MM RESEARCH ORGANIZATION ACQUIRES LICENSE FOR FACTORY COMMANDER™

Specifics on this late breaking news will be updated on WWK's website under "What's New". **http://www.wwk.com**